Dhrystone Performance: Compiler Versions and Ground Rules

Technical note 2018-06-18

Doc. No GRLIB-TN-0015

Issue 1.0

Template: GQMS-TPLT-1-1-0

CHANGE RECORD

Issue	Date	Section / Page	Description
1.0	2018-06-18		First release

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1 INTRODUCTION

1.1 Scope of the Document

This document describes how the Dhrystone benchmark performs on the LEON4 based GR740 processor using different compiler and compiling options.

1.2 Reference documents

[RD1] *Weiss, Alan. "Dhrystone Benchmark: History, Analysis, "Scores" and Recommendations"*

2 DHRYSTONE BENCHMARK

2.1 Overview

Dhrystone is a well-known benchmark intended to represent the integer computing performance of a system [RD1]. When Dhrystone is used, the following "ground rules" are defined:

- Separate compilation
- No procedure merging (no inlining)
- Other optimizations are allowed, but they should be indicated
- Default results are those without "register" declarations (C version)

2.2 Compilation

We want to address the impact of compiler variations and optimizations by compiling different binaries of the same Dhrystone source code that run under the same conditions.

For that purpose, we apply different compiling methods, based on the above mentioned ground rules:

1. Source code compiled separately and inline functions not allowed (ground rules 0)
2. Source code compiled separately and inline functions allowed (ground rules 1)
3. All source code compiled together (ground rules 2).

Ground rules 0 correspond to the original ground rules and the other two are less restrictive versions of them, allowing further optimizations.

In addition to the compilation rules, we use a different optimization level (-O0, -O1, -O2 or -O3) to collect multiple data points depending on the compiler optimization level.

Also, in order to analyse the impact of different compiler versions, we use the following compilers:

- GCC 3.4.4 (BCC 1.0.46)
- GCC 4.4.2 (BCC 1.0.45)
- GCC 4.9.4 (BCC 2.0.0-rc.2-31)
- GCC 7.1.0 (rtems-4.12-rcc-1.3 toolchain with GCC-4.9.4-BCC-2 linker)

In the case of the GR740, the following common compiler options are used:

- For BCC 1:-Wl,-msparcleon0 -mv8
- For BCC 2: -qbsp=gr740 -mcpu=leon3

3 EXECUTION RESULTS

3.1 Overview

To run the binaries, we use a GR-CPCI-GR740 board at 250 MHz system frequency with 64-bit 2*256 MiB PC133 SDRAM at 100 MHz and enabled L2 cache with split transactions.

3.2 Results

The following tables and figure show the obtained performance for each scenario. Tables 1 and 2 show the DMIPS and DMIPS/MHz obtained for each scenario.

Compiler \ Opt. Level	DMIPS (O0)	DMIPS (O1)	DMIPS (O2)	DMIPS (O3)
GCC 3.4.4 (ground rules 2)	114.6	220.3	225.5	304
GCC 4.4.2 (ground rules 2)	112.2	232.9	383.5	459
GCC 4.9.4 (ground rules 2)	116	256.8	362.1	400.8
GCC 7.1.0 (ground rules 2)	117.5	256.5	357.1	463.8
GCC 3.4.4 (ground rules 1)	114.6	220.3	224.4	255
GCC 4.4.2 (ground rules 1)	112.2	232.5	320.5	327.9
GCC 4.9.4 (ground rules 1)	116	234	314.1	322.6
GCC 7.1.0 (ground rules 1)	117.5	235	314	324.7
GCC 3.4.4 (ground rules 0)	114.6	220.3	224.4	225.5
GCC 4.4.2 (ground rules 0)	112.2	232.5	243.6	243.6
GCC 4.9.4 (ground rules 0)	116	223	239.9	239.9
GCC 7.1.0 (ground rules 0)	117	222.7	242.8	242

Table 1: Dhrystone DMIPS compiler comparison on the GR740

Compiler \ Opt. Level	DMIPS/MHz O0	DMIPS/MHz O1	DMIPS/MHz O2	DMIPS/MHz O3
GCC 3.4.4 (ground rules 2)	0.4584	0.8812	0.902	1.216
GCC 4.4.2 (ground rules 2)	0.4488	0.9316	1.534	1.836
GCC 4.9.4 (ground rules 2)	0.464	1.0272	1.4484	1.6032
GCC 7.1.0 (ground rules 2)	0.47	1.026	1.4284	1.8552
GCC 3.4.4 (ground rules 1)	0.4584	0.8812	0.8976	1.02
GCC 4.4.2 (ground rules 1)	0.4488	0.93	1.282	1.3116
GCC 4.9.4 (ground rules 1)	0.464	0.936	1.2564	1.2904
GCC 7.1.0 (ground rules 1)	0.47	0.94	1.256	1.2988
GCC 3.4.4 (ground rules 0)	0.4584	0.8812	0.8976	0.902
GCC 4.4.2 (ground rules 0)	0.4488	0.93	0.9744	0.9744
GCC 4.9.4 (ground rules 0)	0.464	0.892	0.9596	0.9596
GCC 7.1.0 (ground rules 0)	0.468	0.8908	0.9712	0.968

Table 2: Dhrystone DMIPS/MHz compiler comparison on the GR740

Please note that the performance decrease in optimization level 3 between 4.4.2 and 4.9.4 can be explained by a GCC bug (https://gcc.gnu.org/bugzilla/show_bug.cgi?id=64193). This problem is solved in 7.1.0.

Figure 1 represents the results using DMIPS/MHz as the vertical axis of the figure and the compiler optimization level as the horizontal axis.

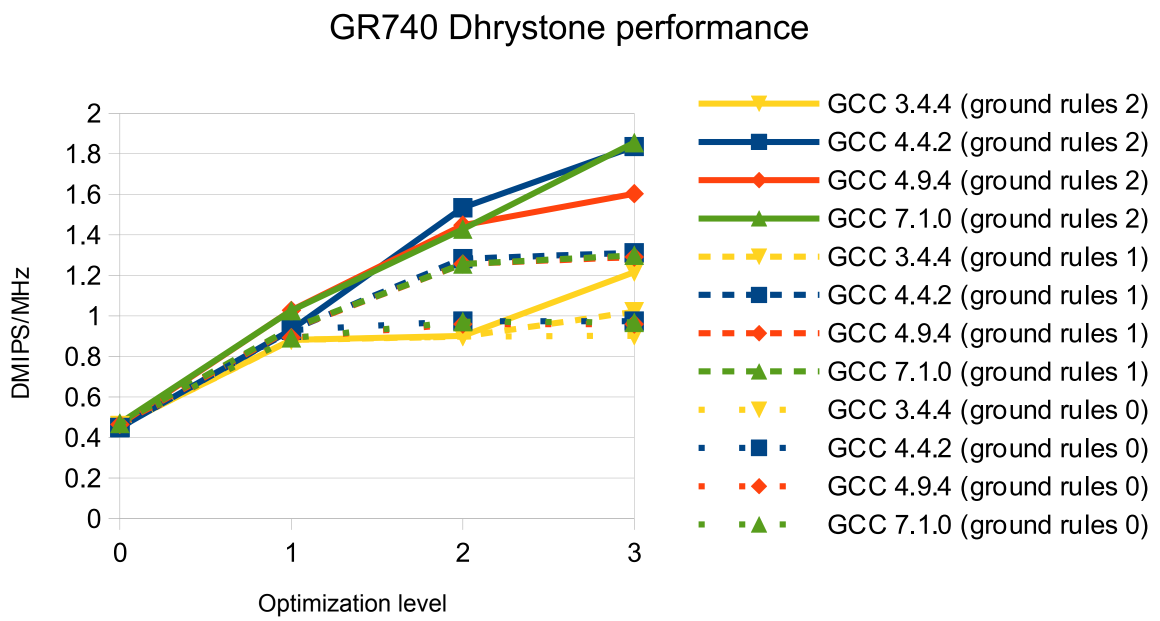

Figure 1: Dhrystone DMIPS/MHz compiler comparison on the GR740

4 CONCLUSION

- Dhrystone performance is affected by which compiler version, optimizations and method is used.
- The default configuration of the GR-CPCI-GR740 development board can achieve up to 463.8 DMIPS (1.8552 DMIP/MHz) on the best scenario.