OCTA-CORE RAD-HARD MICROPROCESSOR

UNDER DEVELOPMENT

GR765

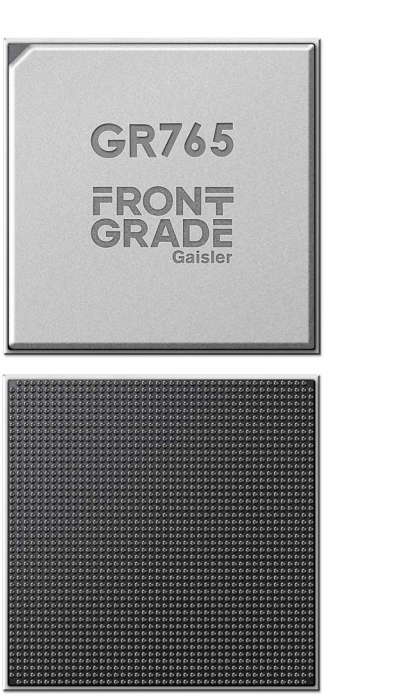
PRODUCT BRIEF

RELEASED APRIL 2026

The GR765 is the next generation radiation-hardened fault-tolerant octa-core microprocessor.

The GR765 brings state-of-the-art capabilities like virtualization, SIMD processing, Gigabit Ethernet, PCIe Gen 3, and SpaceFibre. Additionally, it includes interfaces such as SpaceWire, CAN FD, and MIL-STD-1553B, minimizing the need for external components. An embedded FPGA further enhances the system's flexibility, allowing for custom hardware accelerators and support of bespoke external interfaces without additional external FPGAs for glue logic. Furthermore, the GR765 includes security features such as hardware boot image authentication using post-quantum algorithms, a hardware security module, and several functional security features in the general-purpose processors.

The GR765 provides a mode selection signal that determines at power-up if the device shall have eight LEON5FT SPARC V8 cores or eight NOEL-V RV64GCH cores. This allows one hardware design to take advantage of the strengths from both software ecosystems.



Software Ecosystem

The GR765 benefits from comprehensive support from Frontgrade, including toolchains for operating systems such as Linux, VxWorks, RTEMS, and Zephyr. The partner ecosystem is being expanded to match the level of support provided for previous SoCs like the GR740, with the addition of new software collaborators.

In LEON5 SPARC mode, the GR765 can reuse the qualified software already available for other LEON platforms. When operating in RISC-V mode, the GR765 takes advantage of the growing landscape of open-source tools, libraries, and community-driven developments.

The software ecosystem includes also a bootloader with Standby support (GRBOOT) and an instruction simulator (TSIM).

Development Boards

Frontgrade will at product launch provide two development boards: One development kit that provides access to all interfaces of the GR765, and the GR765-MINI, a compact board intended for software development

Software-enabled features

The GR765 includes a GNSS receiver for the GPS and Galileo constellations. The core can be operated using software libraries provided by Beyond Gravity. The Ethernet switch can be operated as a TTEthernet or TSN switch using software libraries provided by TTTECH.

Debug

GRMON is a debug monitor optimized for the GR765, providing a non-intrusive debug environment. The system can be monitored and controlled by the graphical user interface with scripting support. Furthermore, the RISC-V NOEL-V mode permits use of any debug solution supporting the RISC-V debug specification.

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SPARC RISC-V

Computing

- Radiation-hardened fault-tolerant octa-core architecture
  - Selectable dual-issue processor: LEON5FT SPARC V8 or NOEL-V RISC-V RV64GCH
  - Dedicated FPU and MMU, 32 KiB L1 cache per core connected via multi-port interconnect
  - Packed-SIMD Vector extension on each processor core
  - Support for virtualization and both Type 1 and Type 2 hypervisor usage (MMU and IOMMU with two-stage translation)
  - Proven fault tolerance with hardened flip-flops and error correction on all on-chip and external memories.
- 800 MHz, delivering 2600 DMIPS/core
- 4 MiB L2 8-way cache, 512-bit cache lines
- eFPGA with 30k LUTs
- Hardware authenticated boot (hybrid scheme with ECDSA, ML-DSA)
- Isolated SoC / Hardware Security Module for HW Root of Trust, Secure Boot, Crypto
- DMA controllers

Memory

- DDR2/3/4 interface, 1 chip select, max 16 GiB of accessible memory, configurable as:
  - 96-bit interface with dual x8 device correction capability
  - 80-bit interface with x8 device correction capability
  - 72-bit interface with SECDED
- NAND Flash interface: ONFI 4.0 – NV-DDR2/3 and SDR
  - Supports > 8 Tb without pin-sharing on PCB – more with pin-sharing
- 8/16 bit PROM/IO interface
  - (39/7) BCH EDAC in 8 bit mode
  - boot memory
- QSPI interface
  - max accessible memory 256 MiB
  - boot memory

Interfaces

- PCIe two Gen3 x4 ports, one Gen1 x1 port
- SpaceFibre: 4 ports x1 6.25 Gbit/s + WizardLink support
- SpaceWire router with 12 external interfaces and 4 internal ports
- 4x 10/100/1000 Mbit Ethernet MAC connected to level-2 switch with 6xRGMII or 4xSGMII or 8xQSGMII external Ethernet ports
- 2x MIL-STD-1553B
- 4x CAN FD
- 2x I2C, 12x UART, 2x SPI controller, 48x eFPGA I/O
- SoC Bridge interface
- FPGA Scrubber Controller for external Kintex Ultrascale and Virtex-5
- Debug links:
  - Dedicated: JTAG and SpaceWire
  - CAN, Ethernet

	GR765-AS	GR765-CP
Product Class	Radiation Hardened Flight Model	Engineering Model
Application	Deep Space, GEO, MEO, LEO	Lab Development
Qualification Level	ESCC9030	Not Applicable
Package	FF1760 (45 mm x 45 mm)	FF1760 (45 mm x 45 mm)
TID	50 krad (Si) (guaranteed by platform), 100 krad (Si) (testing/screening to be performed)	Not Applicable
SEL	>= 60 MeV*cm²/mg @ Tj=+125C	Not Applicable
Technology	STM 28nm FDSOI	STM 28nm FDSOI

Security

The GR765 includes an isolated SoC that can be used for system control and security functions acting as a Hardware Security Module (HSM), operating independently from the main system.

Capabilities:

- Authenticated boot for OS and software assets
- Unique device identification
- Hardware-based root of trust
- Secure message signing, verification and encryption
- Key management and cryptographic operations
- Integrated crypto accelerators for performance optimization
- Support for Post-Quantum Cryptography (PQC) algorithms

Firmware:

- Managed by firmware under the system integrator's control
- Example firmware provided with GR765
- Firmware can be customized or replaced with third-party certified solutions

Furthermore, the GR765 features logic for quantum-secure authenticated boot, implemented without any software components. The core combines ECDSA and ML-DSA signature schemes to verify the authenticity and integrity of binary images loaded into the system during the boot sequence.

The architecture includes additional security features such as functional and timing isolation through features in the on-chip interconnect, processor memory management units, and an IO bridge with an IO Memory Management Unit and IO Physical Memory Protection functionality.

In NOEL-V RISC-V mode, the architecture also has support for the RISC-V Control Flow Integrity extensions.

eFPGA

The GR765 includes a radiation-hardened embedded FPGA (eFPGA) with 32k LUTs. Directly interfacing with SpaceFibre and WizardLink communication interfaces, the eFPGA can optimize data decimation tasks and offer efficient in-hardware processing.
The eFPGA is also well-suited for implementing glue logic to connect with custom external interfaces.

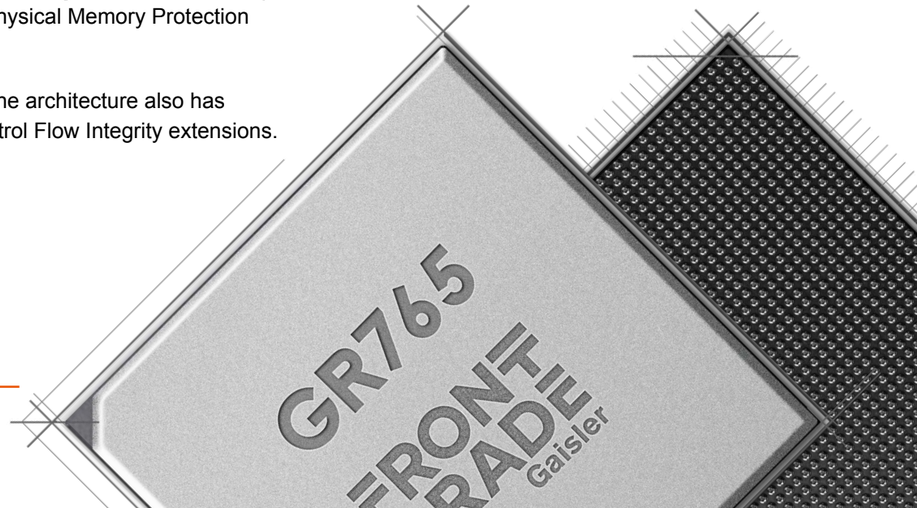
- Configuration memory and registers rad-hard by design
- Built-in configuration memory scrubber
- User memory protected with EDAC

On-chip high-speed memory interconnect

The on-chip striped interconnect between the processor cores and the L2 cache and between the L2 cache and the DDR memory controller allow concurrent accesses to different L2 cache memory banks and DDR memory. This feature increases the bandwidth and minimizes interference between cores.
The system can be configured in an isolated mode that makes use of the dedicated communication channels to remove inter-core interference for memory accesses and simplifies worst-case execution time (WCET) analysis.

SpaceFibre and SpaceWire

The SpaceWire router is also integrated with the SpaceFibre controller. SpaceWire data from/to multiple payloads can be aggregated in a single SpaceFibre High Speed Serial Link without software intervention.



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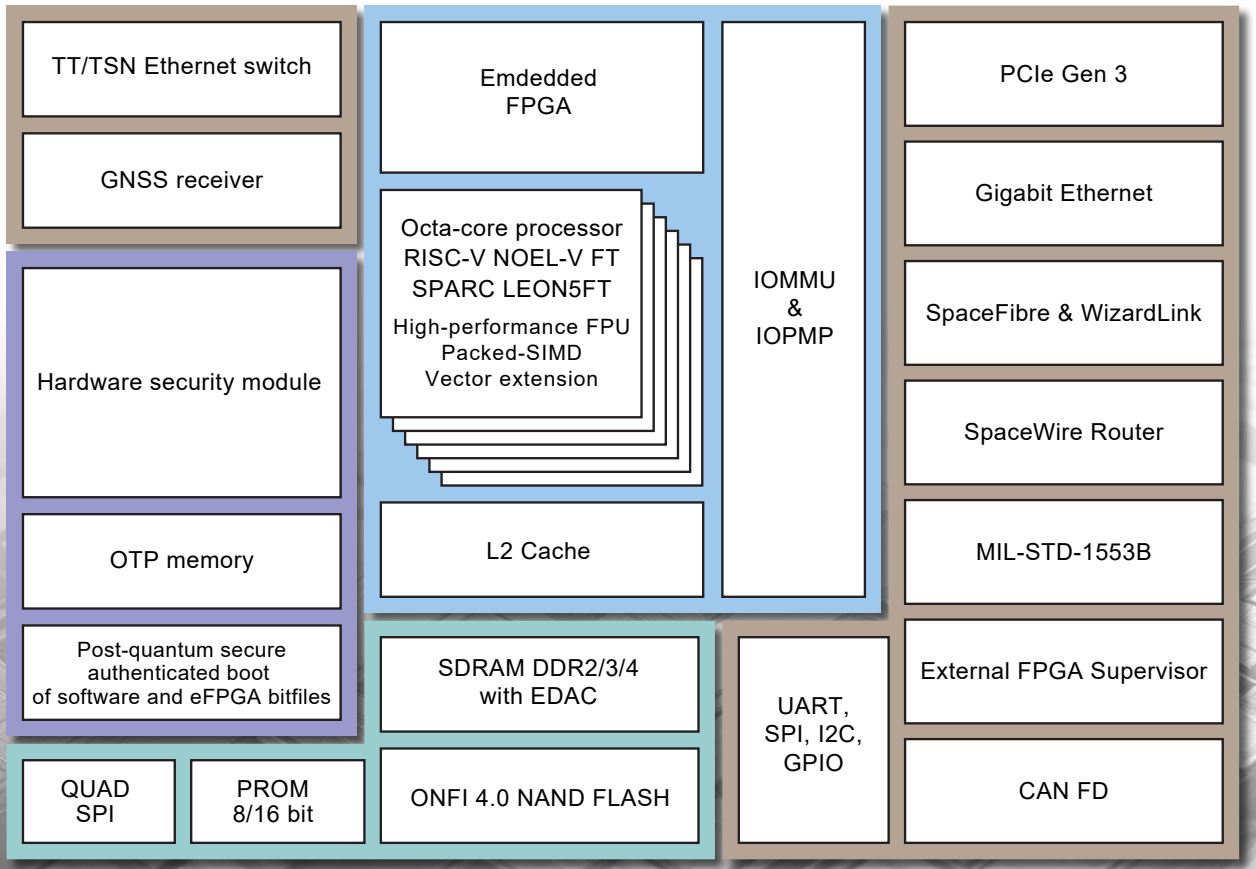
GR765 block diagram



More information:
gaisler.com/GR765

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