OCTA-CORE RAD-HARD MICROPROCESSOR

UNDER DEVELOPMENT

GR765

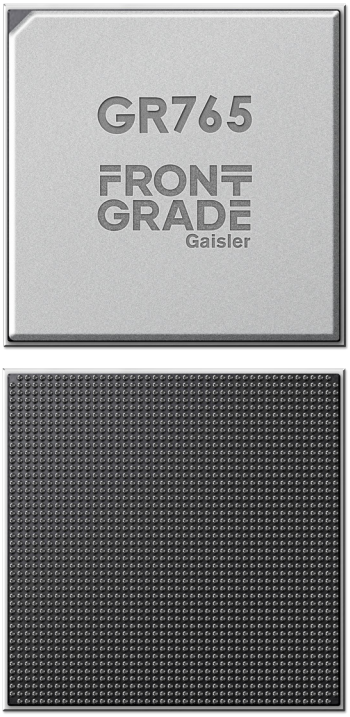
PRODUCT BRIEF

RELEASED MARCH 2025

The GR765 is the next generation radiation-hardened fault-tolerant octa-core microprocessor, introducing advanced features that redefine space processing potential.

The GR765 brings state-of-the-art capabilities like virtualization, SIMD processing, Gigabit Ethernet, PCIe Gen 3, and Space-Fibre. Additionally, it includes interfaces such as SpaceWire, CAN FD, and MIL-STD-1553B, minimizing the need for external components. An embedded FPGA further enhances the system's flexibility, allowing for custom hardware accelerators and support of bespoke external interfaces without additional external FPGAs for glue logic. Furthermore, the GR765 includes security features such as hardware boot image authentication using post-quantum algorithms, a hardware security module, and several functional security features in the general-purpose processors.

The GR765 provides a bootstrap signal that determines at power-up if the device shall have eight LEON5FT SPARC V8 cores or eight NOEL-V RV64GCH cores. This allows one hardware design to take advantage of the strengths from both software ecosystems.



Software Ecosystem

The GR765 is supported by the ecosystem provided by Frontgrade with toolchains for operating systems such as Linux, VxWorks, RTEMS, and Zephyr. The partner ecosystem is also being extended with the same level of support as exists for previous SoCs like the GR740, and with new software partners.

The LEON5 SPARC mode enables re-use of the existing LEON qualified software ecosystem. In RISC-V mode the GR765 can leverage the expanding RISC-V ecosystem providing a wide range of open-source tools, libraries, and community-driven developments.

The software ecosystem includes also a bootloader with Standby support (GRBOOT) and an instruction simulator (TSIM).

Development Boards

Frontgrade will at product launch provide two development boards: One development kit that provides access to all interfaces of the GR765, and the GR765-MINI, a compact board intended for software development

Software-enabled features

The GR765 includes a GNSS receiver for the GPS and Galileo constellations. The core can be operated using software libraries provided by Beyond Gravity. The Ethernet switch can be operated as a TTethernet or TSN switch using software libraries provided by TTtech.

Debug

GRMON is a debug monitor optimized for the GR765, providing a non-intrusive debug environment. The system can be monitored and controlled by the graphical user interface with scripting support. Furthermore, the RISC-V NOEL-V mode permits use of any debug solution supporting the RISC-V debug specification.

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Computing

- Radiation-hardened fault-tolerant octa-core architecture
  - Selectable LEON5FT SPARC V8 or NOEL-V 64-bit RISC-V RV64GCH
  - Dedicated FPU and MMU, 32 KiB L1 cache per core connected via multi-port interconnect
  - Packed-SIMD Vector extension on each processor core
  - Support for virtualization and both Type 1 and Type 2 hypervisor usage (MMU and IOMMU with two-stage translation)
  - Advanced fault-tolerance features, no need for lock-step processing
- 800 MHz, delivering 2600 DMIPS/core
- 4 MiB L2 8-way cache, 512-bit cache lines
- eFPGA with 30k LUTs
- Hardware authenticated boot (hybrid scheme with ECDSA, ML-DSA)
- Isolated SoC / Hardware Security Module for HW Root of Trust, Secure Boot, Crypto
- DMA controllers

Memory

- DDR2/3/4 interface, 1 chip select, max 16 GiB of accessible memory, configurable as:
  - 96-bit interface with dual x8 device correction capability
  - 80-bit interface with x8 device correction capability
  - 72-bit interface with SECDEC
- NAND Flash interface: ONFI 4.0 – NV-DDR2/3 and SDR
  - Supports > 8 Tb without pin-sharing on PCB – more with pin-sharing
- 8/16 bit PROM/IO interface
  - (39/7) BCH EDAC in 8 bit mode
  - boot memory
- QSPI interface
  - max accessible memory 256 MiB
  - boot memory

Interfaces

- PCIe Gen3 controller, 1 port x8, 2 port x4, or 4 port x2 lanes through bifurcation (TBC)
- SpaceFibre: 4 ports x1 6.25 Gbit/s + WizardLink support
- SpaceWire router with 12 external interfaces and 4 internal ports
- 4x10/100/1000 Mbit Ethernet MAC connected to level-2 Ethernet switch with 6x external ports
- 2x MIL-STD-1553B
- 4x CAN FD
- 2x I2C, 12x UART, 2x SPI controller, 48x eFPGA I/O
- SoC Bridge interface
- FPGA Scrubber Controller for external Kintex Ultrascale and Virtex-5
- Debug links:
  - Dedicated: JTAG and SpaceWire
  - CAN, Ethernet

	GR765-AS	GR765-CP
Product Class	Radiation Hardened Flight Model	Engineering Model
Application	Deep Space, GEO, MEO, LEO	Lab Development
Qualification Level	ESCC9030	Not Applicable
Package	FF1924 (45x45 mm)	FF1924 (45x45 mm)
TID	50 krad (Si) (guaranteed by platform), 100 krad (Si) (testing/screening to be performed)	Not Applicable
SEL	78 MeV*cm2/mg @125	Not Applicable
Technology	STM 28nm FDSOI	STM 28nm FDSOI

Security

The GR765 includes an Isolated SoC that can be used for system control and security functions up to providing the whole system with security by acting as a Hardware Security Module (HSM). This isolated subsystem operates independently and communicates with software running on the main system through a mailbox interface. Key features enabled by the system include authenticated boot of Operating System and software assets, unique device identification, hardware-based root of trust, and comprehensive key management and operations. The Isolated SoC supports secure message signing and verification, utilizing both symmetric and asymmetric cryptography, including Post-Quantum Cryptography (PQC). The subsystem include accelerators for crypto applications and the functionality is controlled by firmware that is under control of the system integrator. Example software is provided with the GR765. Application-specific requirements will necessitate firmware changes, with the integrator having the option to develop their own solution or license third-party solutions with security certifications. Furthermore, the GR765 features logic for quantum-secure authenticated boot, implemented without any software components. The core combines ECDSA and ML-DSA signature schemes to verify the authenticity and integrity of binary images loaded into the system during the boot sequence.

The architecture includes additional security features such as functional and timing isolation through features in the on-chip interconnect, processor memory management units, and an IO bridge with an IO Memory Management Unit and IO Physical Memory Protection functionality.

In NOEL-V RISC-V mode, the architecture also has support for the RISC-V Control Flow Integrity extensions.

eFPGA

The GR765 includes a radiation-hardened embedded FPGA (eFPGA) with 32k LUTs. Directly interfacing with SpaceFibre and WizardLink communication interfaces, the eFPGA can optimize data decimation tasks and offer efficient in-hardware processing. The eFPGA is also well-suited for implementing glue logic to connect with custom external interfaces. Being radiation-hardened there is no need to apply Triple Modular Redundancy (TMR) or scrubbing to the eFPGA designs.

On-chip high-speed memory interconnect

The on-chip striped interconnect between the processor cores and the L2 cache and between the L2 cache and the DDR memory controller allow concurrent accesses to different L2 cache memory banks and DDR memory. This feature increases the bandwidth and minimizes interference between cores.
The system can be configured in an isolated mode that makes use of the dedicated communication channels to remove inter-core interference for memory accesses and simplifies worst-case execution time (WCET) analysis.

SpaceFibre and SpaceWire

The SpaceWire router is also integrated with the SpaceFibre controller. SpaceWire data from/to multiple payloads can be aggregated in a single SpaceFibre High Speed Serial Link without software intervention.

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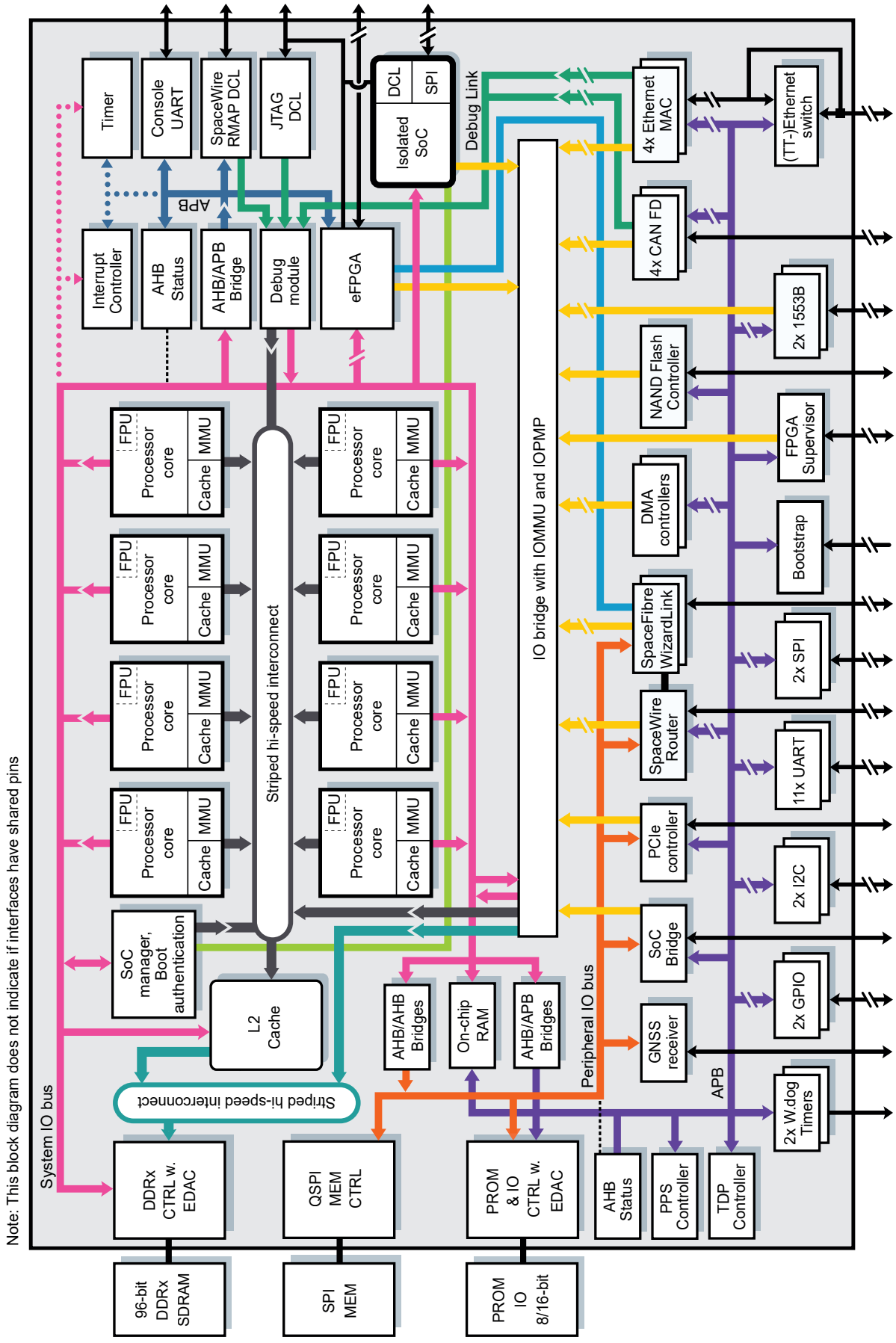

FRONTGRADE Gaisler

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