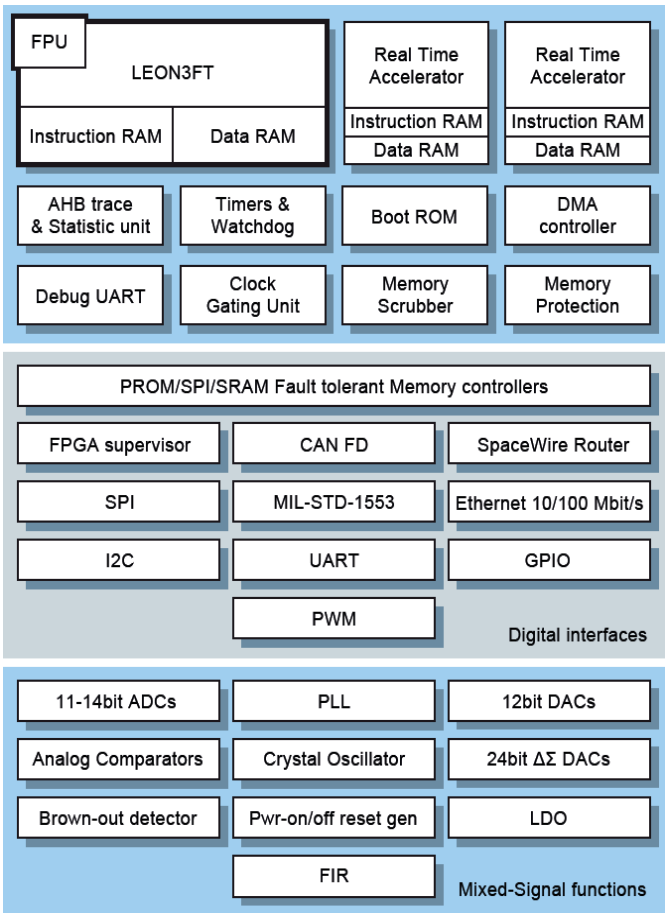
Advanced Data Sheet

LEON3FT Microcontroller
GR716B-PBGA

Features

- Fault-tolerant SPARC V8 processor with 31 register windows, 128KiB EDAC protected tightly coupled memory and support for compressed instruction set
- Double precision IEEE-754 floating point unit
- Memory protection units
- Non-intrusive advanced on-chip debug support unit
- External EDAC protected 8-bit PROM/SRAM, SPI memory protected by EDAC and dual memory redundancy
- Hardware FPGA programming and scrubbing
- Real-Time Accelerators with 64KiB EDAC protected tightly coupled memory, programmable DMA
- SpaceWire router with 2 external ports and time distribution
- MIL-STD-1553B interface
- CAN FD interface with CANOpen support
- PacketWire with CRC acceleration support
- Programmable PWM interface
- Programmable Delta-Sigma modulator DAC
- SPI with SPI-for-Space protocol support
- Four channel 12-bit DAC, four 11-14-bit ADC and twenty fast analog comparators
- 10/100 Ethernet, UARTs, SPI, I^2C, GPIO, Timers with Watchdog, Interrupt controller, UART debug, etc
- Crystal oscillator, with external XTAL
- Precision reference 1.9 V output



Description

The GR716B device is a fault-tolerant LEON3FT SPARC V8 processor with various communication interfaces and on-chip ADC, DAC, Power-on-Reset, Oscillator, Brown-out detection, LVDS transceivers with extended common-mode, cold-spare and fail-safe, regulators to support single 3.3V supply, ideally suited for space and other high-rel applications.

Specification

- System frequency up to 100 MHz
- SpaceWire links up to 100 Mbps
- 400 pins, Plastic Ball Grid Array (PBGA)
- Total Ionizing Dose (TID) guaranteed up to 100 krad (Si)
- Single-Event Latch-up (SEL) immune (LET_{th} > 118 MeV*cm^2/mg)
- Single Event Upset (SEU) proven tolerance with hardened flip-flops and error corrections on all on-chip and external memories
- Support for single 3.3V supply (up to 700 mA core consumption)

Applications

The GR716B microcontroller is an advanced microcontroller, targeting high reliability space and aeronautics applications.

Support for many different standard interfaces makes the GR716B microcontroller ideal for supervision, monitoring and control in a satellite, such as:

- motor control
- program and scrubber support of FPGA
- switching power converters
- power system monitoring and latch-up detection
- magnetorquer control
- remote terminal control unit
- propulsion system control
- sensor bus control
- robotics applications control
- instrument control unit
- antenna pointing control
- nanosatellite controller

Availability

The GR716B microcontroller is currently under validation and there is no guarantee that functionality or performance will not change.

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1 Introduction

1.1 Scope

This document is the advanced data sheet for the GR716B LEON3FT microcontroller. This document provides information regarding the GR716B-PBGA device in the 400-pin plastic ball grid array (PBGA).This document is complemented by the GR716B LEON3FT microcontroller - User's Manual [GR716B-UM], which provides detailed information of processors, analog/digital interfaces and information related to software development. The User manual is common for all versions of GR716B devices.

The GR716B microcontroller has been developed in an activity initiated by the European Space Agency.

1.2 Datasheet limitations

Note that this document is an advanced datasheet:

- Advanced data sheet - Product in development
- Preliminary data sheet - Shipping prototype
- Data sheet - Shipping space-grade product

1.3 Updates and feedback

Updates are available at https://www.gaisler.com/gr716b

Feedback: support@gaisler.com

For commercial questions please contact sales@gaisler.com

1.4 Reference documents

[GRMON4] GRMON4 User's Manual, Frontgrade Gaisler

[SPARC] The SPARC Architecture Manual, Version 8, SPARC International Inc.

[V8E] SPARC-V8 Supplement, SPARC-V8 Embedded (V8E) Architecture Specification, SPARC-V8E, Version 1.0, SPARC International Inc.

[GR716B-UM] GR716B LEON3FT microcontroller - User's Manual, Frontgrade Gaisler, www.frontgrade.com/gaisler

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1.5 Document revision history

Change record information is provided in table 1.

Table 1. Change record

Version	Date	Sections	Note
0.1	November 2025	All sections	Datasheet First release - The previous CQFP Datasheet and User Manual have been split to support PBGA and SiP products. A common User Manual (UM) is now available for all device variants, while each device is provided with its own dedicated Datasheet.

1.6 Acronyms

Table 2. Acronyms

Acronym	Comment
AHB	Advanced High-performance bus, part of [AMBA]
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus, part of [AMBA]
BCH	Bose–Chaudhuri–Hocquenghem, class of error-correcting codes
CAN	Controller Area Network, bus standard
CPU	Central Processing Unit, used to refer to one LEON3FT processor core.
DMA	Direct Memory Access
DSU	Debug Support Unit
EDAC	Error Detection and Correction
FIFO	First-In-First-Out, refers to buffer type
FPU	Floating Point Unit
Gb	Gigabit, 10^9 bits
GB	Gigabyte, 10^9 bytes
GiB	Gibibyte, gigabinary byte, 2^{30} bytes, unit defined in IEEE 1541-200
I/O	Input/Output
ISR	Interrupt Service Routine
JTAG	Joint Test Action Group (developer of IEEE Standard 1149.1-1990)
kB	Kilobyte, 10^3 bytes
KiB	Kibibyte, 2^{10} bytes, unit defined in IEEE 1541-2002
Mb, Mbit	Megabit, 10^6 bits
MB, Mbyte	Megabyte, 10^6 bytes
MiB	Mebibyte, 2^{20} bytes, unit defined in IEEE 1541-2002
MVT	Multi Vector Trapping
PROM	Programmable Read Only Memory
RAM	Random Access Memory
SEE	Single Event Effects
SEL/SEU/ SET	Single Event Latchup/Upset/Transient
SPARC	Scalable Processor ARChitecture
SVT	Single Vector Trapping
SW	Software
UART	Universal Asynchronous Receiver/Transmitter

1.7 Definitions

This section and the following subsections define the typographic and naming conventions used throughout this document.

1.7.1 Bit numbering

The following conventions are used for bit numbering:

- The most significant bit (MSb) of a data type has the leftmost position
- The least significant bit of a data type has the rightmost position
- Unless otherwise indicated, the MSb of a data type has the highest bit number and the LSb the lowest bit number

1.7.2 Radix

The following conventions is used for writing numbers:

- Binary numbers are indicated by the prefix "0b", e.g. 0b1010.
- Hexadecimal numbers are indicated by the prefix "0x", e.g. 0xF00F
- Unless a radix is explicitly declared, the number should be considered a decimal.

1.7.3 Data types

Byte (BYTE)	8 bits of data
Halfword (HWORD)	16 bits of data
Word (WORD)	32 bits of data

2 Electrical description

All electrical specifications are defined at package solder point level, unless otherwise stated.

Specifications in this whole chapter have been derived from simulation of GR716B or validation of GR716A. The GR716B microcontroller is currently in a development phase, and parameter characterization validation and device qualification are yet to be done. All parameter values in this whole chapter are TBC.

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings [1)]

Symbol	Parameter	Rating		Units
		Min.	Max.	
	Voltage between any supply domain grounds [2)]	-0.3	0.3	V
V_{DD_CORE} [5)]	DC Supply for Core	-0.3	2.2 [9) 10)]	V
V_{DD_IO} [5)]	DC Supply for I/O	-0.3	4.0	V
V_{DD_LVDS} [5)]	DC Supply for LVDS I/O	-0.3	4.0	V
V_{DD_LDO} [5)]	DC Supply for LDO	-0.3	V_{DD_IO} +0.3 [8)]	V
V_{DDA} [5)]	DC Supply for Analog domains, except PLL	-0.3	4.0	V
V_{DDA_PLL} [5) 7)]	DC Supply for PLL (supplied from internal LDO)	-0.3	2.2 [10)]	V
V_{GPIO} [5) 12)]	Voltage between GPIO pin and ground	-0.3	V_{DD3V3} +0.3 [8)]	V
V_{DIO_IN} [5) 12)]	Digital CMOS Input voltage	-0.3	V_{DD_IO} +0.3 [8)]	V
V_{DIO_OUT} [5) 12)]	Digital CMOS Output voltage	-0.3	V_{DD_IO} +0.3 [8)]	V
V_{LVDS_IN} [5)]	LVDS Input voltage per pin	-4.5	5.6	V
V_{LVDS_OUT} [5) 13)]	LVDS Output voltage per pin	-0.3	4.0	V
I_{GPIO_IN} [12)]	GPIO current when configured as input or HiZ (ESD-diode current max 10mA)	-10	10	mA
I_{GPIO_OUT} [12)]	GPIO current when configured as output (ESD-diode current max 10mA)	-10	10	mA
I_{DIO_IN} [12)]	Digital Input current (ESD-diode current max 10mA)	-10	10	mA
$I_{DIO\_OUT\_HiZ}$ [12)]	Digital Output current when configured as HiZ (ESD-diode current max 10mA)	-10	10	mA
I_{DIO_OUT} [12)]	Digital Output current when configured as output (ESD-diode current max 10mA)	-10	10	mA
I_{DD_LDO}	LDO current	-10	900 [11)]	mA
Vref [7)]	Bandgap voltage reference	-0.3	V_{DDA} +0.3 [8)]	V
Rref [6)]	Bandgap current reference	-0.3	V_{DDA} +0.3 [8)]	V
Vrefbuf	Reference buffer voltage	-0.3	V_{DDA} +0.3 [8)]	V
Irefbuf	Sourcing current for reference buffer enabled (ESD-diode current max 10mA)	-3	30	mA
C_{RST} [7)]	Reset timing capacitor	-0.3	V_{DD_CORE} + 0.3	V
V_{XO_ANA} [14)]	Crystal oscillator port (pin Y16-Y18)	-0.3	V_{DD_CORE} + 0.3	V

Table 3. Absolute maximum ratings [1)]

Symbol	Parameter	Rating		Units
		Min.	Max.	
T_{store}	Storage Temperature	-40	150	°C
T_j	Junction Temperature		150	°C
Rth,jc	Thermal Resistance, Junction to Case [4)]		4	°C/W
P_D [3)]	Power Dissipation		4	W
V_{HBM}	ESD level		4 [14)]	kV

Note 1: Extended operation at the maximum levels may degrade the performance and affect the reliability of the device. Exceeding the maximum levels may permanently damage the device.

Note 2: Within one and the same supply domain, all GND resp V_{DD} pins must be connected to the same GND resp V_{DD} plane on PCB. Any externally applied voltage difference between GND pins, resp between V_{DD} pins where there are more than one pin per V_{DD} domain, can create harmful circulating ground resp supply currents inside the package.

Note 3: The thermal resistance, Θ_{JC}, sets the maximum power dissipation, P_D, assuming that the package is mounted on PCB with main heat flowing through the main heat-sinking path for the package. Otherwise, maximum power dissipation limit will be significantly lower.

Note 4: Case means bottom of balls, which is the main heat-sink path out of this package.

Note 5: Values are relative to their dedicated supply ground.

Note 6: This pin shall not be connected, except for external resistor to ground.

Note 7: This pin shall not be connected, except for external capacitor to ground.

Note 8: Voltage must not exceed 4.0V

Note 9: Voltage must not exceed V_{DD_LDO} + 0.3V

Note 10: Voltage must not exceed V_{DD_IO} + 0.3V. To guarantee this limit during all kinds of system supply transients (especially rapid unexpected discharge of V_{DD_IO}), a schottky power diode in reverse bias between V_{DD_CORE} and V_{DD_IO} should be considered on PCB. This diode is strongly recommended when V_{DD_CORE} is Externally supplied (V_{DD_LDO} connected to V_{DD_CORE}), and is especially important if total capacitance on V_{DD_CORE} net in the whole power system is large.

Note 11: Repetitive pulse transients must be limited to maximum $1.1A_{Peak}$, with maximum pulse length in the order of 100us. The single pulse transient during LDO start up will not be harmful for the LDO upto the maximum decoupling capacitance on VDD_CORE stated in section 2.2 for single supply mode.

Note 12: All CMOS IO ports are non-cold-spare ports. These inputs and outputs have ESD protection via on-chip diodes to IO ground and IO supply. Forward bias voltage for on-chip ESD protection diodes should not exceed 0.3 V and DC current should not exceed 10mA. For equivalent IO port schematics see section 2.4. For V_{GPIO}, the GPIO port location determines when V_{DD3V3} is V_{DD_IO} or V_{DDA}.

Note 13: V_{LVDS_OUT} is applicable only in LVDS cold-spare mode (V_{DD_LVDS}=-0.1V to 0.2V) and LVDS output-disable mode (V_{DD_LVDS}=3.0V to 3.6V). It is not applicable during the transition V_{DD_LVDS}=0.2V to 3.0V, which is an absolute maximum limitation, meaning that externally applied voltage other than GND onto the LVDS pins must be avoided during this supply transition. I.e., system cold-spare switching of a multi-driver LVDS bus must first power down any active LVDS driver into cold-spare mode, and then power up the one LVDS driver to be active.

The LVDS outputs on pin L14-L17 are non-cold-spare ports and have maximum limits according to GPIO ports, i.e., V_{LVDS_OUT} is not applicable.

Note 14: Crystal oscillator port (pin Y16-Y18) has V_{HBM} of maximum 2kV.

2.2 Recommended operating conditions

Table 4. Recommended operating conditions [1) 2)]

Symbol	Parameter	Rating			Units
		Min.	Typ.	Max.	
	Voltage between any supply domain grounds	-0.1	0.0	0.1	V
V_{DD_CORE} 4) 9)10)	DC Supply for Core f_{intsys} <= 50MHz f_{intsys} <= 100MHz	 1.62 1.71	 1.8 1.9	 1.98 3) 1.98 3)	V
V_{DD_IO} 4)	DC Supply for I/O	3.0	3.3	3.6 3)	V
V_{DD_LVDS} 4) 8)	DC Supply for LVDS I/O	3.0	3.3	3.6 3)	V
V_{DD_LDO} 4) 10)	DC Supply for LDO	3.0	3.3	3.6 3)	V
V_{DDA} 4) 8)	DC Supply for Analog domains, except PLL	3.0	3.3	3.6 3)	V
V_{DDA_PLL} 4) 7)	DC Supply for PLL (supplied from internal LDO)	1.7	1.85	1.98 3)	V
V_{GPIO} 4) 12)	Voltage between GPIO pin and ground	-0.1		V_{DD3V3} +0.1	V
V_{DIO_IN} 4) 12)	Digital CMOS Input voltage	-0.1		V_{DD_IO} +0.1	V
V_{LVDS_IN} 4) 13)	LVDS Input voltage per pin	-4.0 14)		4.5 3)	V
V_{LVDS_OUT} 4) 15)	LVDS Output voltage per pin	-0.1 12)		3.6 3)	V
I_{GPIO_OUT}	GPIO current when configured as output	-5 3)		5 3)	mA
I_{DIO_OUT}	Digital CMOS current when configured as output	-5 3)		5 3)	mA
I_{DD_LDO}	LDO current	0 11)		700 11)	mA
Vref 5)	Bandgap voltage reference		4.7		nF
Rref 6)	Bandgap current reference		5.11		kΩ
Irefbuf	Sourcing current for reference buffer enabled	-1 3)		20 3)	mA
C_{RST} 16)	Reset timing capacitor		100		nF
f_{XO} 17)	Crystal oscillator frequency	5		25	MHz
f_{intsys} 18)	Internal system clock frequency for Core logic	5		100 3)	MHz
f_{extsys}	External input clock frequency for System clock (pin Y12)			100 3)	MHz
f_{extspw} 19)	External input clock frequency for SpaceWire interface and PLL (pin Y10)			100 3)	MHz
SR_{GPIO_IN} 20)	GPIO clock input slew rate	0.5			V/ns
T_{case} 2)	Case Temperature (PBGA)	-40 3)		105 3)	°C

Note 1: Within recommended operating conditions, all functionality and performance parameters in this data-sheet are valid, and device long-term reliability is maintained.

Note 2: Analog performance specifications are guaranteed within -40°C to 110°C junction temperature, unless otherwise stated.

Note 3: To maintain device long-term reliability, this limit must be fulfilled, and Note 8 and Note 12 must be fulfilled where applicable.

Table 4. Recommended operating conditions [1) 2)]

Note 4:	Values are relative to their dedicated supply ground.
Note 5:	Connect 4.7 nF ceramic capacitor to ground, close to the pin with short wire, and not connected to anything else.
Note 6:	Connect 5.11 kΩ ±1%$_{INIT}$ to ground, close to the pin with short wire, and not connected to anything else. The tolerance of this reference resistor will directly affect the accuracy of the DAC outputs. For high-precision DAC applications, a precision resistor should be considered, e.g. ±0.1%$_{INIT}$ ±10 ppm/°C thin metal film type.
Note 7:	The PLL supply voltage, V_{DDA_PLL}, is generated from internal voltage regulator. It shall be decoupled to PLL ground, V_{SSA_PLL}, with ceramic capacitor of about 2 uF (typically 2.2 uF) close to pins with short wires, and V_{DDA_PLL} shall not be connected to anything else.
Note 8:	Any of the supply voltages V_{DDA} or V_{DD_LVDS} can be non-supplied. Then the supply must be grounded via maximum 400 Ω, to maintain device long-term reliability. This is not applicable for V_{DDA_PLL}, where only decoupling capacitor is allowed. For LVDS cold-spare mode, V_{DD_LVDS} must be -0.1 V to 0.2 V(TBD), which is fulfilled when V_{DD_LVDS} is grounded via maximum 400 Ω. When V_{DDA_ADC} is grounded it must be via maximum 200 Ω, and the three on-chip measurement channels into ADC 0-2 respectively must be configured to off state, to maintain device long-term reliability.
Note 9:	The core supply voltage shall be decoupled by typically 10 nF to ground per V_{DD_CORE} and GND pin pair. This supply can be generated from internal voltage regulator, and should then be decoupled also by at least 100 uF damped capacitors (typically 0.1 Ω in series with 100 uF), preferably times two for redundancy.
Note 10:	In single supply mode, V_{DD_LDO} is recommended to be connected to same 3.3 V supply as V_{DD_IO} (for simultaneous ramp up/down), and no external 1.8 V supply shall be connected to V_{DD_CORE}. In single supply mode, the maximum decoupling capacitance on V_{DD_CORE} must not be more than 400 uF (well damped). In dual supply mode, V_{DD_LDO} should be connected to V_{DD_CORE}, and external 1.8 V supply connected to V_{DD_CORE}.
Note 11:	To maintain device long-term reliability, I_{DD_LDO} of maximum 700 mA in average and maximum 1.1 A_{Peak} repetitive pulse transients of maximum length in order of 100 us must be fulfilled. To guarantee full regulation performance of the LDO output voltage (V_{DD_CORE}), maximum 700 mA should be fulfilled. The LDO can supply external 1.8 V loads connected between V_{DD_CORE} and GND on PCB, but these loads must not cause any violations of the above I_{DD_LDO} limits, and must never back-feed any current into the LDO to maintain output voltage regulation and device long-term reliability.
Note 12:	To maintain device long-term reliability, the pin must not be more than 3.6 V from any of its supply rails. Therefore, when pin voltage is at -0.1 V or V_{DD3V3}+0.1 V, the supply voltage V_{DD3V3} must not be higher than 3.5 V. For V_{GPIO}, the GPIO port location determines when V_{DD3V3} is V_{DD_IO} or V_{DDA}. For V_{LVDS_OUT}, the V_{DD3V3} is V_{DD_LVDS}.
Note 13:	Device long-term reliability is maintained for any V_ID that fulfills this voltage range per pin. Extended common mode range is supported in normal operation and cold-spare mode and during transition in-between modes. I.e., the LVDS inputs are also hot-swap compatible, and more than one LVDS input can be active and read across the same 100 Ω receiver termination resistor at the same time.
Note 14:	To maintain device long-term reliability, maximum negative DC voltage on LVDS input pin is -3.6 V_{DC} and transient peak is -4.0 V_{Peak} up to 0.1% duty cycle over lifetime.
Note 15:	V_{LVDS_OUT} is applicable only in LVDS cold-spare mode (V_{DD_LVDS}=-0.1V to 0.2V) and LVDS output-disable mode (V_{DD_LVDS}=3.0V to 3.6V). It is not applicable during the transition V_{DD_LVDS}=0.2V to 3.0V, where externally applied voltage other than GND onto the LVDS pins must be avoided. To maintain device long-term reliability, continuous operation at V_{DD_LVDS}=0.2V to 3.0V is not allowed.
Note 16:	Connect ceramic capacitor to ground, close to the pin with short wire, and not connected to anything else. For functional values see Section 2.11.
Note 17:	For functional configurations of the internal XO, see user manual section 9 [GR716B-UM]. To maintain device long-term reliability, a correct value of R_{X2} must be inserted when applicable, see user manual section 9.2.3 [GR716B-UM].

Table 4. Recommended operating conditions [1) 2)]

Note 18: Outside this frequency range, internal clock detection may switch the internal system clock unconditionally to the external system clock input (pin Y12). To use f_{intsys}<5 MHz, the frequency should be fed into pin Y12 and configured to be used as the internal system clock. See user manual section 4 [GR716B-UM] for clock muxing and configurations.

Note 19: For functional configurations, see chapter 10 [GR716B-UM] for supported PLL input frequencies and user manual section 33 [GR716B-UM] for the SpaceWire interface.

Note 20: This GPIO input slew rate needs to be fulfilled in application cases where GPIO 45, 46, 47, 53 or 61 is configured as clock input, see figure 16 [GR716B-UM]. The reason is that these GPIO inputs are not schmitt trigger inputs. For schmitt trigger clock inputs, there is no minimum limit other than that slew rate must not change sign inside the input switching interval.

2.3 Power supply characteristics

Table 5. DC characteristics [1)]

Symbol	Parameter	Condition	Rating			Units
			Min.	Typ.	Max.	
I_{DD_CORE}	Core Supply current	f_{intsys} = 10 MHz [2) 3)]		150	TBD	mA
		f_{intsys} = 100 MHz [2) 3)]		1200	TBD	mA
I_{DD_LDO}	LDO Supply current	f_{intsys} = 10 MHz [2) 3)]		155	TBD	mA
I_{DD_IO}	I/O Supply current	f_{intsys} = 100 MHz [2) 3) 4)] Excluding I/O output current. PLL, ADC and ACOMP disabled. LVDS ports (pin L14-L17) enabled.		20	TBD	mA
		I/O and LVDS ports (pin L14-L17), PLL, ADC and ACOMP disabled.		0.1	TBD	mA
I_{DDA_PLL}	PLL Supply current	Internally supplied from V_{DD_IO}		10	TBD	mA
I_{DDA} + $I_{DD\_IO\_ANA}$	Sum of Analog Supply currents	Analog functions operational: $4xI_{DAC} + 4xI_{ADC} + 20xI_{ACOMP} + I_{REF}$ Excluding I/O and V_{RefBuf} output current.		70	TBD	mA
I_{DD_LVDS}	LVDS I/O Supply current	Operational [4)] Shutdown [4)]		40 0.01	TBD TBD	mA

Note 1: Recommended operating conditions, see chapter 2.2

Note 2: Digital user scenario with CAN and SpaceWire running at full data rate.

Note 3: LEON3 and 2xRTA running 100% (with frequent memory access), internal SpaceWire clock at 100 MHz.

Note 4: Valid signals applied on LVDS inputs, and 100 Ω differential terminations on LVDS outputs. Valid signals applied on CMOS inputs, and no external load on CMOS outputs.

2.4 Simplified schematics for IO buffers

Simplified input and output buffer schematics presented in this chapter are applicable within absolute maximum rating conditions, see chapter 2.1

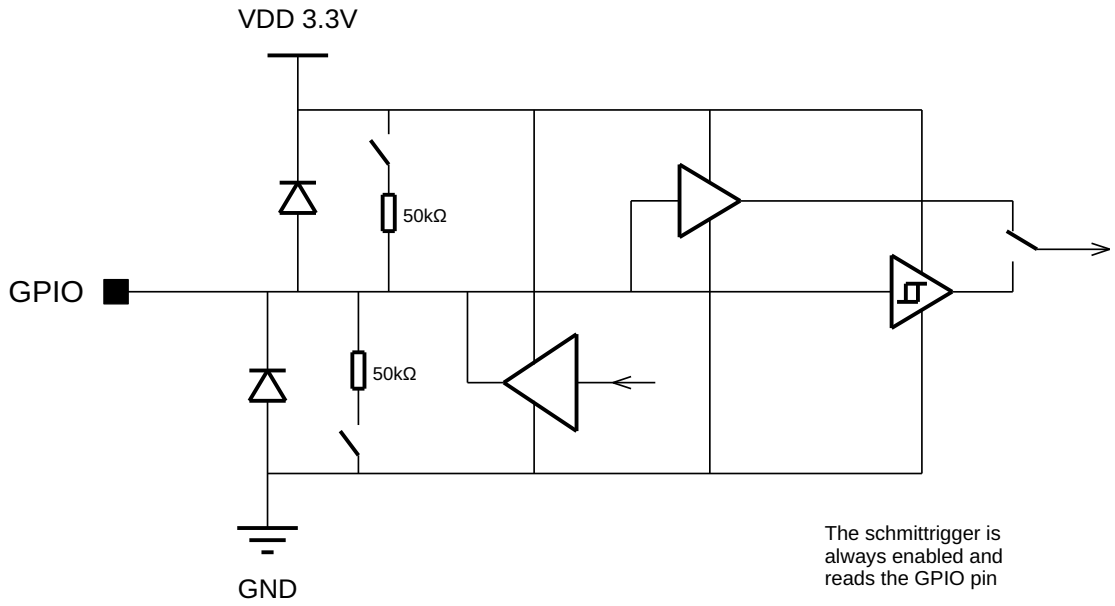

Figure 1. Simplified schematic of Bidirectional Digital GPIO buffer

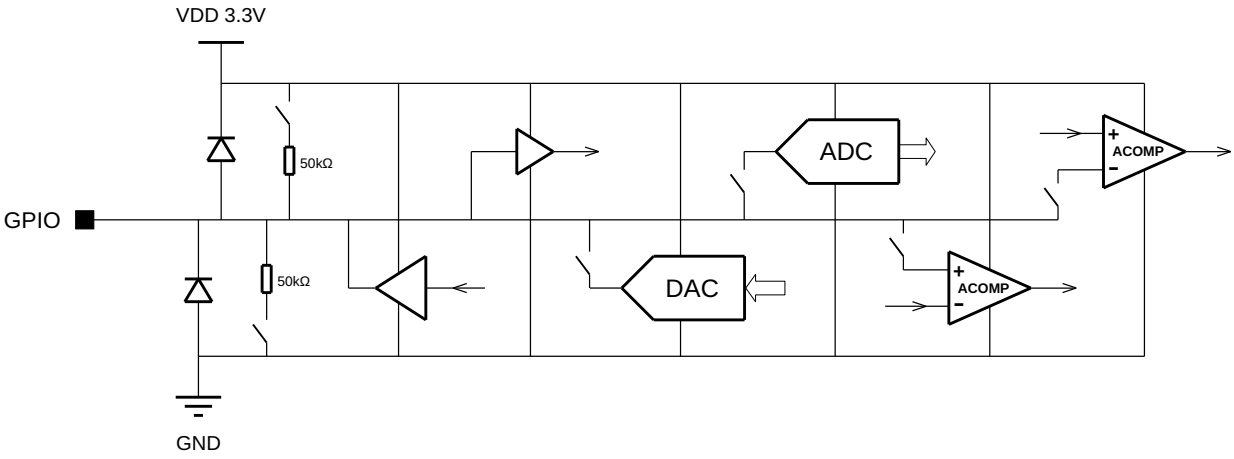

Figure 2. Simplified schematic of Bidirectional GPIO buffer with Analog capabilities

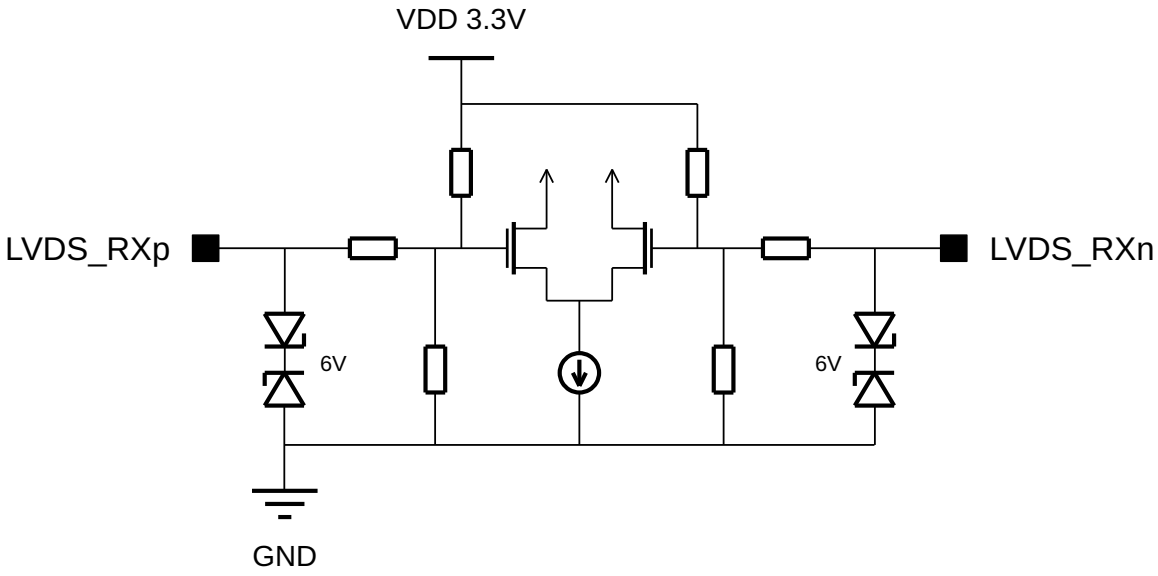

Figure 3. Simplified schematic of LVDS input buffer with Cold-Spare support

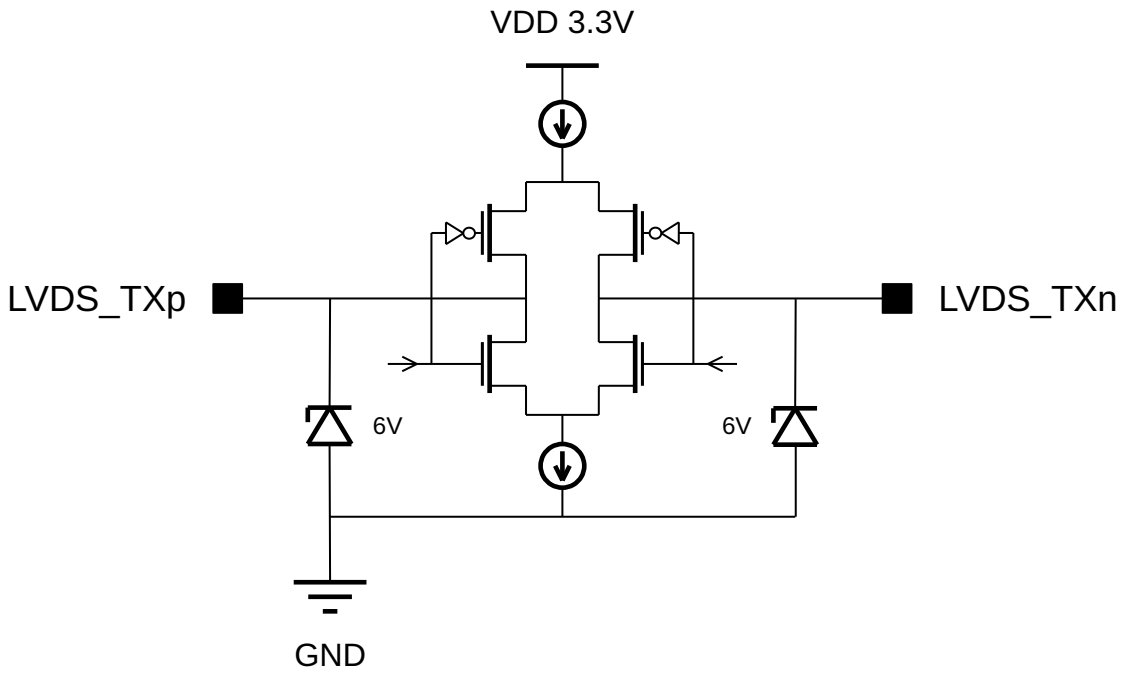

Figure 4. Simplified schematic of LVDS output buffer with Cold-Spare support

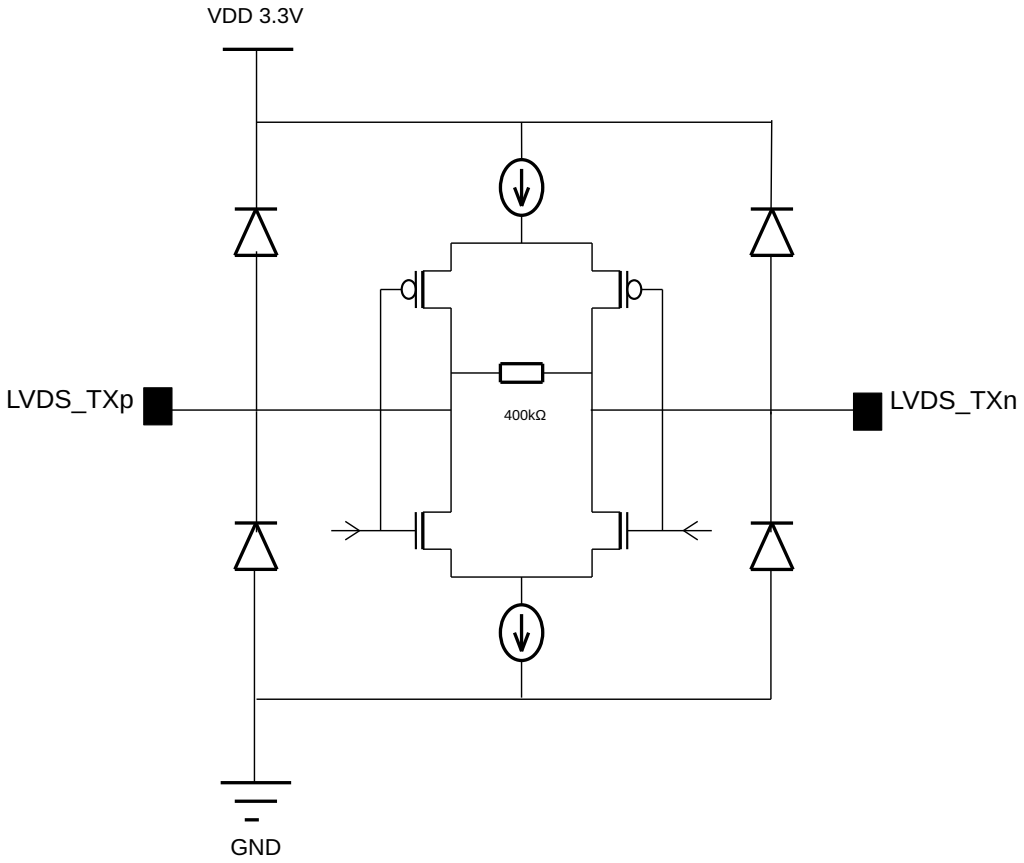

Figure 5. Simplified schematic of LVDS non-cold-spare output buffer

2.5 Input voltages, leakage currents and capacitances

Table 6. DC characteristics for CMOS inputs [1)]

Symbol	Parameter	Condition	Rating			Units
			Min.	Typ.	Max.	
V_{IH}	Input High Voltage CMOS		0.67x V_{DD_IO}			V
V_{IL}	Input Low Voltage CMOS				0.27x V_{DD_IO}	V
V_{IH_SCH} [9)]	Input High Voltage Schmitt trigger		0.75x V_{DD_IO}			V
V_{IL_SCH} [9)]	Input Low Voltage Schmitt trigger				0.23x V_{DD_IO}	V
V_{I_HYST}	Input Hysteresis Voltage Schmitt trigger		0.1	0.2	0.3	V
I_{ILEAK_1} [3)]	Input Leakage Current GPIO	$V_{IN} = V_{DD\_IO}$			3	uA
		V_{IN} = 2.6 V [10)]	-0.7		0.7	uA
		V_{IN} = -0.1 V	-0.7			uA
		V_{IN} = -0.1 V to 2.6 V @TBD °C [12)]	-0.15		0.15	uA
I_{ILEAK_2} [3)]	Input Leakage Current GPIO with int. pull down	$V_{IN} = V_{DD\_IO}$			100	uA
		V_{IN} = 0 V	-1			uA
I_{ILEAK_3} [3)]	Input Leakage Current GPIO with int. pull up	$V_{IN} = V_{DD\_IO}$			1	uA
		V_{IN} = 0 V	-100			uA
I_{ILEAK_PUD} [3) 11)]	Input Leakage Current during power up/down GPIO 0-36, 63	V_{DD_IO} = 0V-3.6V V_{DD_CORE}= 0V-1.98V <V_{DD_IO} V_{IN} = -0.1V to V_{DD_IO}+0.1V	-10 [2)]		10 [2)]	uA
		V_{DD_CORE} = 0V-1.98V $V_{DD\_IO} = V_{DD\_CORE}$ $V_{IN} = V_{DD\_IO}$ / 2	-10		10	uA
		V_{DD_CORE} = 0V-1.98V V_{DD_IO} = 3.0V, 3.6V $V_{IN} = V_{DD\_IO}$ / 2	-10		10	uA
		V_{DD_IO} = 0V-3.6V $V_{DD\_LDO} = V_{DD\_IO}$ V_{DD_CORE} supplied by LDO $V_{IN} = V_{DD\_IO}$ / 2	-10		10	uA
I_{ILEAK_4} [4)]	Input Leakage Current CMOS with int. pull down	$V_{IN} = V_{DD\_IO}$			160	uA
		V_{IN} = 0 V	-1			uA
I_{ILEAK_5} [5)]	Input Leakage Current CMOS	$V_{IN} = V_{DD\_IO}$			5	uA
		V_{IN} = 0 V	-5			uA
I_{ILEAK_6} [6)]	See Note 6					
I_{ILEAK_7} [7)]	Input Leakage Current Internal pull down	$V_{IN} = V_{DD\_IO}$			320	uA
		V_{IN} = 0 V	-3			uA
I_{ILEAK_8} [8)]	Input Leakage Current Internal pull up	$V_{IN} = V_{DD\_IO}$			1	uA
		V_{IN} = 0 V	-160			uA

Table 6. DC characteristics for CMOS inputs [1)]

C_{IO}	Input Capacitance				5 [2)]	pF

Note 1: Recommended operating conditions, see chapter 2.2

Note 2: Guaranteed by design. Not tested in production.

Note 3: GPIO port configured to HiZ/input mode, and programmable analog functions disabled.

Note 4: CLK, SPWCLK, DUART_RX, DSU_EN and DSU_BREAK input only.

Note 5: SPIM_SEL, SPIM_SCK and SPIM_MOSI input only.

Note 6: I_{ILEAK_6} is for RESET_IN_N input only, and it is presented in table 15.

Note 7: TESTEN input only.

Note 8: SPIM_MISO input only.

Note 9: Input pins with schmitt trigger are listed in table 37. The input voltage is allowed to be at any level from -0.1V to V_{DD_IO}+0.1V continuously, where device long-term reliability is maintained upto 110ºC for any intermediate input level. When it is between V_{IL_SCH} and V_{IH_SCH}, the supply current, I_{DD_IO}, is increased up to 4.5 mA per input. For GPIO ports to operate in this input interval, the GPIO should be configured to Analog mode. An input must not be more than 3.6 V from any of its supply rails to maintain device long-term reliability, so when it is at -0.1V or V_{DD_IO}+0.1V, the supply voltage must not be higher than 3.5 V.

Note 10: Guaranteed by production measurement for GPIO 37-48 and 51-58. Guaranteed by design for the other GPIO ports.

Note 11: For I_{ILEAK_PUD} to be applicable, the V_{DD_CORE} and V_{DD_IO} maximum slewrate needs to be ±10 V/ms, and the GPIO port must be configured to HiZ/input mode. During power supply ramp up, this GPIO mode is guaranteed by the internal power-on reset. During supply ramp down it needs to be configured from User software before the ramp down starts, or at the latest in an interrupt routine triggered by the Brown-out detector on V_{DD_CORE}, V_{DD_IO} or V_{DDA_REF} (internal critical references), whichever that triggers its Brownout level first. Other Brownout detectors for critical supplies should also be included, such as for the PLL if the internal system clock comes from the PLL. Finally, also before supply ramp down, all software execution on GR716 should be suspended into halt state by clock gating, to avoid faulty register writings from erroneous execution when V_{DD_CORE} falls below recommended operating conditions.

Note 12: Guaranteed by design. Not tested in production. Valid for GPIO 37, 38, 41, 43, 44, 45, 46, 47, 51, 52, 55, 56, 57, 58.

Table 7. Characteristics for LVDS inputs [1) 2)]

Symbol	**Parameter**	**Condition**	**Rating**			**Units**
			Min.	**Typ.**	**Max.**	
V_{TH}	Differential positive threshold		10	40	90 [7)]	mV
V_{TL}	Differential negative threshold		-90 [7)]	-40	-10	mV
V_{T_HYST}	Differential threshold hysteresis		40	80	180 [7)]	mV
$\|V_{ID}\|$	Differential input magnitude	Bitrate 0.1 Mbit/s: 50 Mbit/s: 100 Mbit/s: 200 Mbit/s:	 0.1 0.1 0.15 0.2		 2.0 2.0 2.0 2.0	V
V_{ECMR} [4)]	Extended common mode range	$\|V_{ID}\|$ 0.1 V : 2.0 V :	 -3.95 [5)] -3.00 [5)]		 4.45 3.50	V
I_{I_LVDS}	Input current per pin	V_{LVDS_IN} 0V to 2.4V : -4.0V to 5.0V :	 -20 -30 [4)]		 20 30 [4)]	uA

Table 7. Characteristics for LVDS inputs [1) 2)]

Symbol	Parameter	Condition	Rating			Units
			Min.	Typ.	Max.	
I_{IB}	Input balance current		-6		6	uA
C_{I_LVDS}	Input capacitance per pin				5 [3)]	pF
t_{fsa}	Failsafe activation delay	$\|V_{ID}\| < 25$ mV	100		1000	ns
t_{fsd}	Failsafe deactivation delay	$\|V_{ID}\|$ goes to normal operation	5 [3)]		50 [3)]	ns
SR_{ID}	Differential slewrate		2 [3) 6)]			V/us

Note 1: Recommended operating conditions, see chapter 2.2

Note 2: Compliant to ANSI TIA/EIA-644 “Low Voltage Differential Signaling”

Note 3: Guaranteed by design. Not tested in production.

Note 4: Extended common mode range is supported in normal operation and cold-spare mode and during transition in-between modes. I.e., the LVDS inputs are also hot-swap compatible, and more than one LVDS input can be active and read across the same 100ohm receiver termination resistor at the same time.

Note 5: Maximum negative DC voltage per pin is -3.6 V_{DC} and transient peak is -4.0 V_{Peak} up to 0.1% duty cycle over lifetime, to maintain device longterm reliability.

Note 6: Limited by the failsafe activation delay.

Note 7: Extended common-mode operation defines this limit.

2.6 Output voltages, leakage currents and capacitances

Table 8. DC characteristics for Digital CMOS outputs [1)]

Symbol	Parameter	Condition	Rating			Units
			Min.	Typ.	Max.	
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA [3)]	V_{DD_IO} - 0.5			V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA [3)]			0.4	V
I_{OLEAK}	Output Leakage Current	Outputs at tri-state. $V_{OUT} = V_{DD\_IO}$ and V_{OUT}=0V	-10		10	uA
C_{IO}	Output Capacitance				5 [2)]	pF

Note 1: Recommended operating conditions, see chapter 2.2

Note 2: Guaranteed by design. Not tested in production.

Note 3: Digital CMOS outputs have 2mA drive capability, except for DUART_TX (pin D3) and XO_OUT (pin Y14) which have drive capability of and are tested at 4mA. See also Table 37.

Table 9. DC characteristics for LVDS outputs in the V_{DD_LVDS} supply domain [1) 2)]

Symbol	Parameter	Condition	Rating			Units
			Min.	Typ.	Max.	
V_{OS}	Offset voltage	[4)]	1.125	1.250	1.375	V
ΔV_{OS}	Change in magnitude of V_{OS} for complementary output states	[4)]	-50		50	mV
$\|V_{OD}\|$	Absolute differential Output voltage	[4)]	250	350	450	mV
$\Delta\|V_{OD}\|$	Change in magnitude of $\|V_{OD}\|$ for complementary output states	[4)]	-50		50	mV
I_{OZ} [5)]	Output leakage current when disabled	V_{LVDS_OUT} = -0.1V to 3.6V V_{DD_LVDS} = 3.0V to 3.6V	-2		2	uA
I_{OZ_OFF} [5)]	Output leakage current in power off (cold-spare mode)	V_{LVDS_OUT} = -0.1V to 3.6V V_{DD_LVDS} = -0.1V to 0.2V	-2		2	uA
I_{OS}	Short-circuit Output current			6	12	mA
I_{ODS}	Differential short-circuit Output current			4	12	mA
C_{O_LVDS}	Output capacitance per pin				5 [3)]	pF

Note 1: Recommended operating conditions, see chapter 2.2

Note 2: Compliant to ANSI TIA/EIA-644 “Low Voltage Differential Signaling”. The Symbols/Parameters are defined in this standard.

Note 3: Guaranteed by design. Not tested in production.

Note 4: LVDS outputs are terminated with 100Ω differentially.

Table 9. DC characteristics for LVDS outputs in the V_{DD_LVDS} supply domain [1) 2)]

Note 5: Applicable in LVDS cold-spare and output-disable mode, respectively, but not applicable *during supply transition* in-between these modes.

Table 10. DC characteristics for LVDS outputs on GPIO ports [1) 2) 3)]

Symbol	Parameter	Condition	Rating			Units
			Min.	Typ.	Max.	
V_{OS}	Offset voltage	5)	1.125	1.250	1.375	V
ΔV_{OS}	Change in magnitude of V_{OS} for complementary output states	5)	-50		50	mV
$\|V_{OD}\|$	Absolute differential Output voltage	5)	250	350	450	mV
$\Delta\|V_{OD}\|$	Change in magnitude of $\|V_{OD}\|$ for complementary output states	5)	-50		50	mV
I_{OZ}	Output leakage current when disabled	6)	-2		2	uA
I_{OS}	Short-circuit Output current				12	mA
I_{ODS}	Differential short-circuit Output current				12	mA
C_{O_LVDS}	Output capacitance per pin				5 [4)]	pF

Note 1: Recommended operating conditions, see chapter 2.2

Note 2: Compliant to ANSI TIA/EIA-644 “Low Voltage Differential Signaling”. The Symbols/Parameters are defined in this standard.

Note 3: These LVDS outputs are non-cold-spare ports. The LVDS output pin voltage must be between GND and V_{DD_IO}, otherwise the on-chip ESD protection diodes will conduct current.

Note 4: Guaranteed by design. Not tested in production.

Note 5: LVDS outputs are terminated with 100 Ω differentially.

Note 6: Each LVDS pair is internally connected with a differential resistor (~400 kΩ). The given output leakage currents only apply with the opposite LVDS output terminal floating.

2.7 DAC Electrical Characteristics

Table 11. Electrical characteristics for DAC outputs

Symbol	Parameter	Condition	Rating			Units
			Min.	Typ.	Max.	
	Resolution			12		Bit
f_S	Sampling rate	Full analog performance: Full functionality: f_S is user programmable (f_{intsys} divided by even integer > 2).			3 [1) 3)] 25 [3)]	MSps
FS	Fullscale current	I_{Rref} = Vref/Rref = 1.000V/5.11kΩ		4.00		mA
FS_{ERR}	Fullscale error	Excluding Vref and Rref tolerances	-1		1	%
I_{OFFS}	Offset current		-0.5		0.5	LSB
INL	Integral non-linearity	With DEM: Without DEM:			2 [2)] 3 [2)]	LSB
DNL	Differential non-linearity	With DEM: Without DEM:			1 [2)] 1.5 [2)]	LSB
V_{OUT}	Compliance voltage		-0.1 [5)]		V_{DDA}-0.7 [4)]	V
PSRR	Power supply rejection ratio	V_{DDA} = 3.3V_{DC} ±0.3V_{DC}: V_{DDA} = 20mV_{pp} , 100kHz:			1 [1)] 1 [1)]	uA_{pp}
$\|I_{OUT\_SD}\|$	Output leakage current	Shutdown. V_{OUT} = -0.1V to 2.6V		0.01	0.7	uA
I_{DDA}	Current consumption per DAC	Operational, f_S=25MSps, with DEM: Shutdown:		5 0.001	6 0.01	mA
V_{DDA}	Supply voltage		3.0		3.6	V

Note 1: Guaranteed by design. Not tested in production.

Note 2: A 1 nF ceramic capacitor to V_{SSA_DAC} placed very close to the GPIO pin is required. It will low-pass filter charge ejection from the internal DAC current switching, which is especially important in the continuously switching DEM mode. These parameters are tested in production at TBD MSps, at V_{OUT} = -0.1 V and V_{DDA}-0.7 V.

Note 3: Max 3MSps, with load impedance to ground of 500 Ω and 100 pF, give large-signal settling to 0.1%. Max 25MSps is allowed on DAC digital input, which may not give full analog settling between samples but can give smoother waveforms when generating analog ramps, etc.

Note 4: Analog performance not guaranteed for V_{OUT}>2.6 V.

Note 5: The DAC output voltage must not be more than 3.6 V from any of its supply rails, to maintain device long-term reliability. When output voltage is -0.1 V, the supply voltage must not be higher than 3.5 V.

2.8 ADC Electrical Characteristics

Table 12. Electrical characteristics for ADC inputs

Symbol	Parameter	Condition	Rating			Units
			Min.	Typ.	Max.	
	Resolution	User programmable conversion mode Mode 0: Mode 1: Mode 2: Mode 3: Differential and Single-ended analog input mode.		**11** **14** **15** [2] **16** [2]		Bit
f_S	Sampling rate	Mode 0: Mode 1: Mode 2: Mode 3: One MUX input channel at a time. * At minimum t_{track} and t_{conv}			500 * 312 * 128 * 80 *	kSps
$f_{adc,clk}$	Clock input frequency	Single-ended input. $f_{adc,clk}$ is user programmable (f_{intsys} divided by integer > 1).			10	MHz
		Differential input. $f_{adc,clk}$ is user programmable (f_{intsys} divided by integer >1).			5	MHz
t_{track}	Track time	Mode 0: Mode 1: Mode 2: Mode 3:	0.6 0.8 1.0 1.0		400 [1) 3)] 50 [1) 3)] 25 [1) 3)] 25 [1) 3)]	us
t_{conv}	Conversion time excluding track time	Single-ended input. Mode 0: Mode 1: Mode 2: Mode 3: * At maximum $f_{adc,clk}$	1.3 * 2.3 * 6.9 * 11.5 *		200 [1) 4)] 50 [1) 4)] 25 [1) 4)] 25 [1) 4)]	us
		Differential input. Mode 0: Mode 1: Mode 2: Mode 3: * At maximum $f_{adc,clk}$	2.6 * 4.6 * 13.8 * 23.0 *		200 [1) 4)] 80 [1) 4)] 40 [1) 4)] 40 [1) 4)]	us
I_{DD} [6)]	Current consumption per ADC, including pre-amplifier	Shutdown		0.1	10	uA
V_{DD} [6)]	Supply voltage		3.15		3.6	V
Single-ended analog input (always without pre-amplifier)						
FS	Fullscale	Vref=1.000V V_{SSA_REF} is reference for ADC 0-2. GND is reference for ADC 3.		2.5		V

Table 12. Electrical characteristics for ADC inputs

Symbol	Parameter	Condition	Rating			Units
			Min.	Typ.	Max.	
FS_{ERR}	Fullscale error	Excluding Vref tolerances	-0.5		0.5	%
V_{INOFFS}	Offset voltage	Mode 0: Mode 1: Mode 2: Mode 3:	-1 TBD TBD TBD		1 TBD TBD TBD	mV
INL	Integral non-linearity	Mode 0: Mode 1: Mode 2: Mode 3:			2 TBD TBD TBD	mV
DNL	Differential non-linearity	Mode 0: Mode 1: Mode 2: Mode 3:			1.5 TBD TBD TBD	mV
C_{IN}	Input capacitance	Unselected channel: Selected channel during Track:		 28	5 [1] 35 [1]	pF
PSRR [6]	Power supply rejection ratio	V_{DD} = 3.3V_{DC} ±0.3V_{DC}: V_{DD} = 20mV_{pp} , 100kHz:			1 [1] 1 [1]	mV
I_{DD} [6]	Current consumption per ADC, excluding pre-amplifier	Operating at $f_{S,max}$ and $f_{adc,clk,max}$		10	TBD	mA
Differential analog input, without pre-amplifier						
FS_{diff}	Fullscale	Vref=1.000V		±2		V
$FS_{diff,ERR}$	Fullscale error	Excluding Vref tolerances	-0.5		0.5	%
V_{INOFFS}	Offset voltage	Mode 0: Mode 1: Mode 2: Mode 3:	-1.5 TBD TBD TBD		1.5 TBD TBD TBD	mV
INL	Integral non-linearity	Mode 0: Mode 1: Mode 2: Mode 3:			1.5 TBD TBD TBD	mV
DNL	Differential non-linearity	Mode 0: Mode 1: Mode 2: Mode 3:			1 TBD TBD TBD	mV
C_{IN}	Input capacitance per pin	Unselected channel: Selected channel during Track:		 28	5 [1] 35 [1]	pF
CMRR [6]	Common mode rejection ratio	Vin+ and Vin- within 0.4V to 2.6V TBC			1 [1]	mV
		20mV_{pp} , 100kHz			1 [1]	
PSRR [6]	Power supply rejection ratio	V_{DD} = 3.3V_{DC} ±0.3V_{DC}: V_{DD} = 20mV_{pp} , 100kHz:			1 [1] 1 [1]	mV
I_{DD} [6]	Current consumption per ADC, excluding pre-amplifier	Operating at $f_{S,max}$ and $f_{adc,clk,max}$		10	TBD	mA
Pre-amplifier differential analog input (used with ADC differential mode)						

Table 12. Electrical characteristics for ADC inputs

Symbol	Parameter	Condition	Rating			Units
			Min.	Typ.	Max.	
G_{PreAmp}	Gain of Pre-Amp	Gain x1 Gain x2 Gain x4		1 2 4		
$G_{PA,ERR}$	Gain error of Pre-Amp	Independent error per input channel	-0.5 [1)]		0.5 [1)]	%
$V_{PA,OFFS}$	Input offset voltage of pre-amp, excluding ADC offset.	Gain x1 Gain x2 Gain x4	-0.5 [1)] -0.5 [1)] -0.5 [1)]		0.5 [1)] 0.5 [1)] 0.5 [1)]	mV
$R_{IN,DM}$	Input resistance, differential mode, for selected channel during Track.	Gain x1 Gain x2 Gain x4		84 56 33		kΩ
$R_{IN,CM}$	Input resistance, common mode, for selected channel during Track.	Gain x1 Gain x2 Gain x4		84 [5)]		kΩ
C_{IN}	Input capacitance per pin				5 [1)]	pF
CMR [6)]	Input common mode range	Gain x1	TBD		TBD	V
		Gain x2	TBD		TBD	
		Gain x4	TBD		TBD	
CMRR [6)]	Input-referred common mode rejection ratio	Within full CMR_{DC}: $20mV_{pp}$, 100kHz:			1 [1)] 1 [1)]	mV
PSRR [6)]	Input-referred power supply rejection ratio	$V_{DD} = 3.3V_{DC} \pm 0.3V_{DC}$: $V_{DD} = 20mV_{pp}$, 100kHz:			1 [1)] 1 [1)]	mV
I_{DD} [6)]	Current consumption per ADC, including pre-amplifier	Operating at $f_{S,max}$ and $f_{adc,clk,max}$		12	TBD	mA

Note 1: Guaranteed by design. Not tested in production.

Note 2: This conversion mode provides single event transient (SET) detection status flag.

Note 3: This is maximum track time in pre-amplifier mode to maintain full accuracy up to 110°C. At 125°C, performance degradation of hundreds of microvolt may be expected, but maximum track time can be shortened a factor of two or preferably three to minimize this degradation. In by-pass mode, there is no maximum track time limit.

Note 4: This is maximum ADC conversion time, excluding track time, to maintain full accuracy up to 110°C. At 125°C, performance degradation of a couple of LSB may be expected, but maximum conversion time can be shortened a factor of two or preferably three to minimize this degradation.

Note 5: CM impedance is defined as small-signal current per input pin, when applying CM small-signal voltage. The internal CM termination DC voltage is 1.5 V.

Note 6: Supply voltage, V_{DD}, for ADC 0-2 is V_{DDA_ADC} vs V_{SSA_ADC}, and for ADC 3 it is V_{DD_IO} vs GND.

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2.9 Analog Comparator Electrical Characteristics

Table 13. Electrical characteristics for Analog Comparator inputs

Symbol	Parameter	Condition	Rating			Units
			Min.	Typ.	Max.	
$V_{IN,SW}$	Differential input voltage for output switching	Including offset and hysteresis	-13	+/-4	13	mV
$V_{IN,HYST}$	Differential input hysteresis		5	8	11	mV
t_{resp}	Response time	Fast mode				ns
		Differential overdrive 50mV:	7	12	18	
		Differential overdrive 15mV:	15	30	45	
		Disturbance tolerant mode				
		Differential overdrive 50mV:	35	55	80	
		Differential overdrive 15mV:	45	70	95	
t_{rej}	Pulse rejection time	**Disturbance tolerant** mode. Differential square pulse -50mV → 1V → -50mV 50mV → -1V → 50mV	20	35	50	ns
CMR [3]	Input common mode range		-0.1 [2]		V_{DD} -0.9 [2]	V
CMRR [3]	Input common mode rejection ratio		30 [1]			dB
PSRR [3]	Power supply rejection ratio		30 [1]			dB
I_{DD} [3]	Current consumption per comparator	Operational:		400	500	uA
		Shutdown:		0.01	1	
V_{DD} [3]	Supply voltage		3.0		3.6	V

Note 1: Guaranteed by design. Not tested in production.

Note 2: One comparator input outside CMR, with the other input inside CMR or outside in opposite direction, will still guarantee correct comparator functionality, guaranteed by design not tested in production. An input that is more than 0.1V outside its supply rails does not guarantee electrical characteristics such as leakage current. The input is not allowed to be more than 3.6V from any of its supply rails to maintain device long-term reliability. If any input is subjected to repetitive current pulses through any of its on-chip ESD diodes, schottky diode(s) from the input to the supply rail(s) is needed.

Note 3: Supply voltage, V_{DD}, for comparator 0-11 is V_{DDA_ADC} vs V_{SSA_ADC}, and for comparator 12-19 it is V_{DD_IO} vs GND.

2.10 Reference Voltages and Currents Electrical Characteristics

Table 14. Reference Voltages and Currents Electrical characteristics

Symbol	Parameter	Condition	Rating			Units
			Min.	Typ.	Max.	
$Vref_{DC}$	Reference voltage	Room temperature	0.980 [7]	1.008	1.035 [7]	V
		10 - 85 °C	-0.5 [1]		0.5 [1]	%
		-55 - 110 °C	-1 [7]		1 [7]	
		Aging drift [4]	-0.2 [5]		0.2 [5]	
		TID drift	-0.3 [6]		0.3 [6]	
$Vref_{Noise}$	Reference noise	Integrated noise. 4.7nF on Vref pin to V_{SSA_REF}		20		uV_{rms}
$PSRR_{Vref}$	Power supply rejection ratio	$V_{DDA} = 3.3V_{DC} \pm 0.3V_{DC}$: $V_{DDA} = 20mV_{pp}$, 100kHz:			0.6 [1] 1 [1]	mV_{pp}
I_{Rref}	Reference current	5.11kΩ$_{typ}$ on Rref pin to V_{SSA_REF} $I_{Rref,typ} = Vref_{DC,typ} / Rref_{typ}$	[2]	197	[2]	uA
t_{start}	Start-up time, after V_{DDA} is operational	4.7nF on Vref pin to V_{SSA_REF}		0.2	0.5 [1]	ms
Reference buffer output						
$Vrefbuf_{Gain}$	Reference buffer gain	Vrefbuf output voltage = $Vrefbuf_{Gain}$ x Vref		1.9		
		Tolerance at room temperature	-0.3 [1] [7]		0.3 [1] [7]	%
		Total tolerance over -55 - 110 °C	-0.5 [1] [7]		0.5 [1] [7]	
$\|\Delta Vrefbuf\|_{Load}$	Output load regulation	$\|\Delta Irefbuf\| = 1mA_{DC}$ and $\|dIrefbuf/dt\| < 0.1mA/us$			0.1 [1]	mV
$Vrefbuf_{Noise}$	Output noise	Integrated noise. 4.7nF on Vref pin to V_{SSA_REF}		150		uV_{rms}
Irefbuf	Output sourcing current		-1		20	mA
$t_{settling}$ [3]	Output settling time	Residual settling voltage 1 mV : 0.1 mV :			 2 [1] 3 [1]	us
ACOMP internal reference levels (supplied by ADC supply domain)						
VrefACOMP-Gain	ACOMP reference voltage levels (x7)	VrefACOMP reference voltage = $VrefACOMP_{Gain}$ x Vref		0 0.125 0.25 0.5 1 1.5 2		
		Tolerance at room temperature	-0.3 [1] [7]		0.3 [1] [7]	%
		Total tolerance over -55 - 110 °C	-0.5 [1] [7]		0.5 [1] [7]	
Power supply for Reference generation and Reference buffer amplifier						
I_{DDA_REF}	Current consumption	Excluding Vrefbuf output current		2	4	mA
V_{DDA_REF}	Supply voltage		3.0		3.6	V

Note 1: Guaranteed by design. Not tested in production.

Note 2: Determined by the total tolerance spread of Rref pin external resistor and Vref.

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Table 14. Reference Voltages and Currents Electrical characteristics

Note 3:	Settling after start-up from power down, after fast load step of |ΔIrefbuf|<21mA, or after other environmental transient disturbances. The transient disturbance peak voltage may be in the order of $1V_{Peak}$. After LP filter on PCB of 330 Ω_{min} and 120 nF_{min} , or 470 Ω_{nom} and 100 nF_{nom} , the environmental disturbance transients should be <1 mV_{Peak}. After LP filter of 330 Ω_{min} and 1.2 uF_{min} , or 470 Ω_{nom} and 1 uF_{nom} , they should be <0.1 mV_{Peak}.
Note 4:	4000 hours at 125°C and V_{DDA_REF} = 3.6 V
Note 5:	Start of aging drift is applicable after 240 hours burn-in at 125°C. Without burn-in, the aging drift can be -1.2% / +0.4%.
Note 6:	Total Ionizing Dose (TID) test to 100 krad(Si).
Note 7:	$Vref_{DC}$ is verified in production by measurement on Vrefbuf output (at Irefbuf=0).

2.11 Reset and Brownout Detector Electrical Characteristics

Table 15. Reset Electrical Characteristics

The on-chip power on reset generator creates a reset signal that is fed to the rest of the system. This reset signal, POR_INT_N, is asynchronous. It activates the internal reset and has a delayed release controlled by an external capacitance, C_RST. The POR_INT_N and RESET_IN_N are logically *and* gated, and generates internal reset, which is synchronously released after this delay.

Symbol	Parameter	Condition	Rating			Units
			Min.	Typ.	Max.	
t_{RLS} 2) 3) 4)	Release delay, for internal power-on reset signal POR_INT_N	C_{RST} = 0: C_{RST} = 1 nF: C_{RST} = 100 nF: The delay starts at $V_{DD,RST,TH}$ crossing during V_{DD_CORE} ramp up.	 0.2 20	0.1 0.5 50	 1.4 140	ms
t_{RSP} 1)	Response delay, for internal power-on reset signal POR_INT_N	C_{RST} = 0: C_{RST} = 1 nF: C_{RST} = 100 nF: The delay starts at $V_{DD,RST,TL}$ crossing during V_{DD_CORE} ramp down.		1 TBD TBD		us
$V_{DD,RST,TH}$	Reset high threshold for V_{DD_CORE} 5)		1.2	1.4	1.6	V
$V_{DD,RST,TL}$	Reset low threshold for V_{DD_CORE} 5)		1.1	1.3	1.5	V
$V_{DD,RST,HYST}$	Reset hysteresis for V_{DD_CORE} 5)		50	100	150	mV
$V_{IN,RST,TH}$	Input high threshold for RESET_IN_N 6)	V_{DD_CORE} according to table 4	0.5	0.9	1.3	V
$V_{IN,RST,TL}$	Input low threshold for RESET_IN_N 6)	V_{DD_CORE} according to table 4	0.4	0.7	1.0	V
$V_{IN,RST,HYST}$	Input hysteresis for RESET_IN_N 6)	V_{DD_CORE} according to table 4	50	200	350	mV
I_{ILEAK_6}	Input leakage for RESET_IN_N 6)	V_{IN} = V_{DD_IO} : V_{IN} = 0 V :	5 -30		30 -5	uA
I_{DD}	Current consumption			150	350	uA
V_{DD_CORE}	Supply voltage and reset detection voltage		-0.1		2.0	V

Note 1: Guaranteed by design. Not tested in production.

Note 2: For power-on reset to function properly with specified release delay, t_{RLS}, first V_{DD_CORE} must be discharged and stay below 0.2 V for at least a time of $t_{RLS,min}$.

Note 3: Production tested in dual and single supply mode. In single supply mode, tested for default setting of internal LDO.

Note 4: Reset timing external capacitor, C_{RST}, must be large enough to keep the device in reset until all power supplies and the system clock are stable. The reset release time, t_{RLS}, can be estimated by:
$t_{RLS,typ}$ = 0.5 ms/nF*C_{RST}
For example t_{RLS_100nF} = 0.5 ms/nF*100 nF = 50 ms_{typ}. There is no maximum limit for C_{RST} value, but the required discharge time will increase proportionally, see $t_{RLS,min}$ in Note 2. If C_{RST} pin would be left open, i.e., C_{RST}=0, then t_{RLS} will be in the order of 0.1 ms, but that is not recommended due to disturbance risk from other PCB circuitry. Therefore it is recommended to always connect at least 1 nF to this pin.

Table 15. Reset Electrical Characteristics

Note 5:	The reset threshold for V_{DD_CORE} is generated by an independent voltage reference in this internal power-on reset block.
Note 6:	The RESET_IN_N input pin is 3.6 V tolerant, and has no ESD protection diode to any positive supply. It has weak pull-up of 100 kΩ to V_{DD_CORE}.

Table 16. Characteristics for 1.8 V Brownout Detector

Symbol	Parameter	Condition	Rating			Units
			Min.	Typ.	Max.	
V_{TH} 2)	Threshold	Settings in 25mV steps				V
		000 | 111		1.600 | 1.775		
		Threshold Detector	-1 1)		1 1)	%
		Initial tol. at room temp. for Vref : Drift over full temp. for Vref :	-3 1) 3) -1 1) 3)		3 1) 3) 1 1) 3)	
t_{RSP}	Response time		2 1)		30 1)	us
I_{DD}	Current consumption per Brownout block	Operational: Shutdown:		25 0.01	50 1	uA
V_{DD_BO}	Supply voltage and Brownout detection voltage		1.5		2.0	V

Note 1: Guaranteed by design. Not tested in production.

Note 2: All Brownout Detectors use the Vref pin reference to generate the trig thresholds, so the Vref tolerances are to be added to the threshold detector tolerance. Also the internal LDOs for V_{DD_CORE} and V_{DDA_PLL} use the Vref pin reference. This means that the Vref tolerances are common for the Brownout Detectors and V_{DDA_PLL}, and for V_{DD_CORE} in single-supply mode. Hence, tolerance or drift of Vref will not give Brownout trig or affect any trig voltage margins.

Note 3: $Vref_{DC}$ is verified in production by measurement on Vrefbuf output.

Table 17. Characteristics for 3.3V Brownout Detector

Symbol	Parameter	Condition	Rating			Units
			Min.	Typ.	Max.	
V_{TH} 2)	Threshold	Settings in 50 mV steps				V
		000 | 111		2.90 | 3.25		
		Threshold Detector	-1 1)		1 1)	%
		Initial tol. at room temp. for Vref : Drift over full temp. for Vref :	-3 1) 3) -1 1) 3)		3 1) 3) 1 1) 3)	
t_{RSP}	Response time		2 1)		30 1)	us
I_{DD}	Current consumption per Brownout block	Operational: Shutdown:		50 0.01	100 1	uA
V_{DD_BO}	Supply voltage and Brownout detection voltage		2.7		3.6	V

Note 1: Guaranteed by design. Not tested in production.

Table 17. Characteristics for 3.3V Brownout Detector

Symbol	Parameter	Condition	Rating			Units
			Min.	Typ.	Max.	

Note 2: All Brownout Detectors use the Vref pin reference to generate the trig thresholds, so the Vref tolerances are to be added to the threshold detector tolerance.

Note 3: $Vref_{DC}$ is verified in production by measurement on Vrefbuf output.

2.12 Core Supply LDO Electrical Characteristics

Table 18. Characteristics for Core Supply LDO

Symbol	Parameter	Condition	Rating			Units
			Min.	Typ.	Max.	
V_{OUT} [2]	LDO output voltage, internally connected to V_{DD_CORE}	I_{OUT} = 0 Settings in ca 25mV steps.				V_{DC}
		011 * 010 001 000 111 110 101 100 * Default setting after Reset		1.92 1.90 1.87 1.85 1.83 1.80 1.78 1.75		
		Tolerance at room temperature: Temperature drift:	-3 [1] -1 [1]		3 [1] 1 [1]	%
$\Delta V_{OUT,Load}$	Load regulation	I_{OUT} = 700 mA_{DC}	-0.14	-0.07		V_{DC}
I_{OUT}	LDO output current	Sum of supply currents internally to V_{DD_CORE} and externally to loads connected between V_{DD_CORE} and GND on PCB.	0 [3]		700 [3]	mA_{DC}
I_{DD_LDO}	Current consumption	I_{OUT} = 0		2		mA
V_{DD_LDO} [4]	Supply voltage		3.0		3.6	V

Note 1: Tested in production for setting 011b (1.92 V) and 100b (1.75 V). Accuracy for the other settings is guaranteed by design, and these levels are functionally tested to provide stepwise decreasing voltage from 1.92 V down to 1.75 V.

Note 2: The LDO regulates V_{OUT} based on the Vref pin reference.

Note 3: To maintain device long-term reliability, I_{OUT} of maximum 700 mA in average and maximum 1.1 A_{Peak} in repetitive pulse transients of maximum length in order of 100 µs must be fulfilled. To guarantee full regulation performance of the output voltage, V_{OUT}, maximum 700 mA should be fulfilled. The LDO can supply external 1.8 V loads connected between V_{DD_CORE} and GND on PCB, but these loads must not cause any violations of the above I_{OUT} limits, and must never back-feed any current into the LDO to maintain output voltage regulation and device long-term reliability.

Note 4: When the LDO is not used, V_{DD_LDO} should be connected to V_{DD_CORE}, and external supply is connected to V_{DD_CORE}.

2.13 AC characteristics

Timing figures provided in this section are guaranteed by functional testing or measurements, unless otherwise noted.

All measured AC parameters are tested with capacitive load with at least 25 pF on the outputs. Timing measurements will be performed using a voltage level equivalent to $V_{DD\_IO}/2$.AC characteristics presented in this chapter is applicable within recommended operating conditions, see section 2.2

2.13.1 System clock timing

The timing waveforms are shown in figure 6, and the timing parameters are defined in table 19.

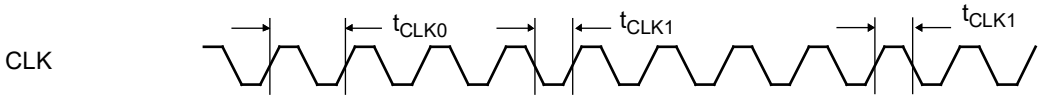

Figure 6. System clock timing waveforms

Table 19. System clock timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{CLK0}	Clock period	-	10	1)	ns
t_{CLK1}	Clock high/low pulse length	-	0.40 x t_{CLK0}	0.60 x t_{CLK0}	ns
t_{CLK2}	Clock cycle jitter 2)	-	-	1	ns

Note 1: Max value can not be larger than 8 x clock period of internal SpaceWire clock when SpaceWire is used.

Note 2: This is guaranteed by design.

2.13.2 External SpaceWire clock timing

The timing waveforms are shown in figure 7, and the timing parameters are defined in table 20.

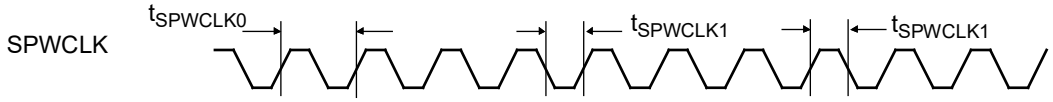

Figure 7. External SpaceWire clock timing waveforms

Table 20. External SpaceWire clock timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{SPWCLK0}$	Clock period 1)	-	5 4)	-	ns
	Clock period 2) 3)	-	10	200	ns
$t_{SPWCLK1}$	Clock high/low pulse length 1) 5)	-	0.45 x $t_{SPWCLK0}$	0.55 x $t_{SPWCLK0}$	ns
	Clock high/low pulse length 2) 5)	-	0.40 x $t_{SPWCLK0}$	0.60 x $t_{SPWCLK0}$	ns
$t_{SPWCLK2}$	Clock cycle jitter 1) 5)	-	-100	100	ps
	Clock cycle jitter 2) 5)	-	-	1	ns

Note 1: Only applicable when PLL is bypassed (see user manual section 4 [GR716B-UM]).

Note 2: Only applicable when PLL use SPWCLK to generate internal SpaceWire clock (see user manual section 4 [GR716B-UM]).

Note 3: If internal SpaceWire clock come from PLL then it cannot be set higher than 100 MHz.

Table 20. External SpaceWire clock timing parameters

Note 4:	Min values given here is from static timing analysis, in production test lowest value used is 10 ns TBC.
Note 5:	This is guaranteed by design.

2.13.3 External 1553B clock timing

The timing waveforms are shown in figure 8, and the timing parameters are defined in table 21.

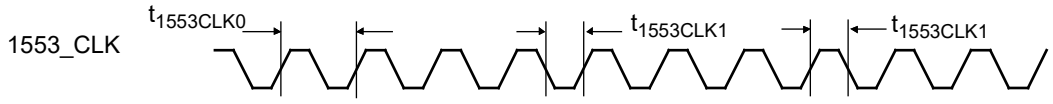

Figure 8. External 1553B clock timing waveforms

Table 21. External 1553B clock timing parameters

Name	Parameter	Reference edge	Typ	Unit
$t_{1553CLK0}$	Clock period	-	50	ns
$t_{1553CLK1}$	Clock high/low pulse length	-	25	ns

Note 1:	External MIL-1553B clock is only available via IO mux, see user manual section 2.5 [GR716B-UM].
Note 2:	Max value of t_{CLK0} cannot be larger than 2 x clock period of internal 1553B clock when 1553B is used.

2.13.4 External SPI4S clock

The timing waveforms are shown in figure 9, and the timing parameters are defined in table 22.

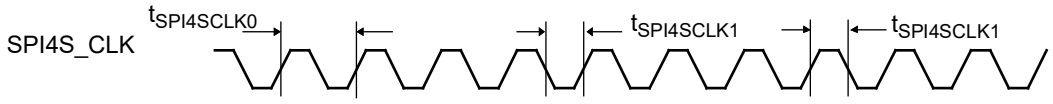

Figure 9. External SPI4S clock timing waveforms

Table 22. External PacketWire clock timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{SPI4SCLK0}$	Clock period	-	40 [3]		ns
$t_{SPI4SCLK1}$ [2]	Clock high/low pulse length	-	0.40 x $t_{SPI4SCLK0}$	0.60 x $t_{SPI4SCLK0}$	ns
$t_{SPI4SCLK2}$ [2]	Clock cycle jitter	-	-100	100	ps

Note 1:	External SPI4S clock is only available via IO mux, see user manual section 2.5 [GR716B-UM].
Note 2:	This is guaranteed by design.
Note 3:	Min values given here is from static timing analysis, in production test lowest value used is TBC ns.

2.13.5 Reset timing

The timing waveforms are shown in figure 10, and the timing parameters are defined in table 23. See user manual section 8 [GR716B-UM] for further information on RESET_IN_N and RESET_OUT_N.

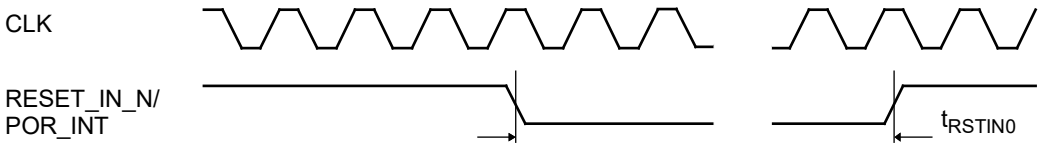

Figure 10. Reset timing waveforms

Table 23. Reset timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{RSTIN0}	Asserted period	-	10 x t_{CLK0} [2) 3)]	-	ns
Note 1:	The RESET_IN_N input is re-synchronized internally, and does not have to meet any setup or hold requirements.				
Note 2:	V_{DD_CORE} must reach at least minimum operating voltage before start for t_{RSTIN0} before RESET_IN_N is de-asserted.				
Note 3:	The internal reset for the system clock domain is released 30 x t_{CLK0} after RESET_IN_N is de-asserted. The internal reset for the SpaceWire clock domain is released 5 internal SpaceWire clock cycles after internal reset is de-asserted and PLL has acquired lock.				
Note 4:	POR_INT is an internal signal from the on-chip POR circuit.				
Note 5:	This parameter is functional tested, and min time is guaranteed by design.				

2.13.6 SPI Master and Memory interface timing

The timing waveforms are shown in figure 11, and the timing parameters are defined in table 24.

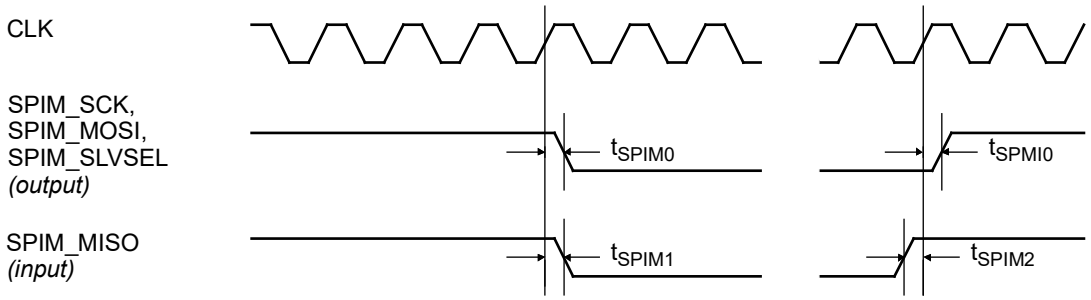

Figure 11. SPI interface timing waveforms

Table 24. SPI interface timing parameters

Name	**Parameter**	**Reference edge**	**Min**	**Max**	**Unit**
t_{SPIM0} [2)]	Clock to output delay	Rising CLK edge	0	45	ns
t_{SPIM1} [2)]	Input to clock hold	Rising CLK edge	-	4	ns
t_{SPIM2} [2)]	Input to clock setup	Rising CLK edge	-	4	ns
Note 1:	The SPI_MISO input is re-synchronized internally, and does not have to meet any setup or hold requirements.				
Note 2:	Verified by static timing analysis, not tested in production.				

2.13.7 SPI Slave interface timing

The timing waveforms are shown in figure 11, and the timing parameters are defined in table 25.

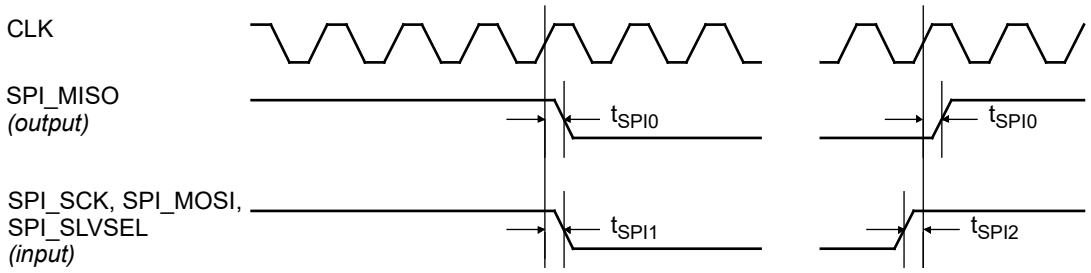

Figure 12. SPI interface timing waveforms

Table 25. SPI interface timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{SPI0} 2)	Clock to output delay	Rising CLK edge	0	45	ns
t_{SPI1} 2)	Input to clock hold	Rising CLK edge	-	4	ns
t_{SPI2} 2)	Input to clock setup	Rising CLK edge	-	4	ns

Note 1: The SPI_SCK, SPI_MOSI and SPI_SLVSEL inputs are re-synchronized internally, and does not have to meet any setup or hold requirements.

Note 2: Verified by static timing analysis, not tested in production.

2.13.8 SPI4S Slave interface CMOS timing

The timing waveforms are shown in figure 11, and the timing parameters are defined in table 26.

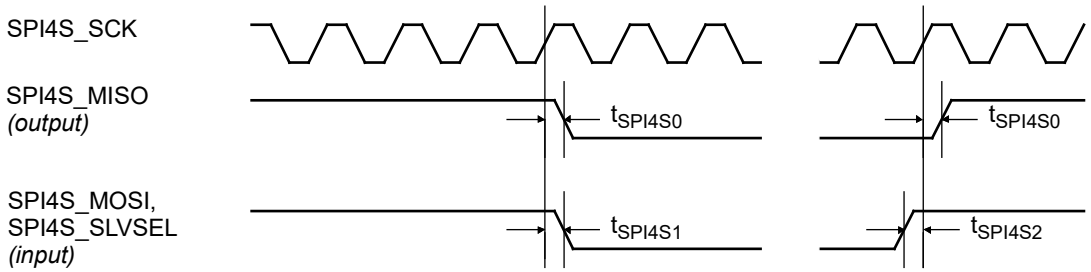

Figure 13. SPI interface timing waveforms

Table 26. SPI interface timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{SPI4S0}	Clock to output delay	Rising SPI4S_CLK edge	0	45	ns
t_{SPI4S1} 1)	Input to clock hold	Rising SPI4S_CLK edge	-	4	ns
t_{SPI4S2} 1)	Input to clock setup	Rising SPI4S_CLK edge	-	4	ns

Note 1: Verified by static timing analysis, not tested in production.

2.13.9 SPI4S Slave interface LVDS timing

The timing waveforms are shown in figure 11, and the timing parameters are defined in table 27.

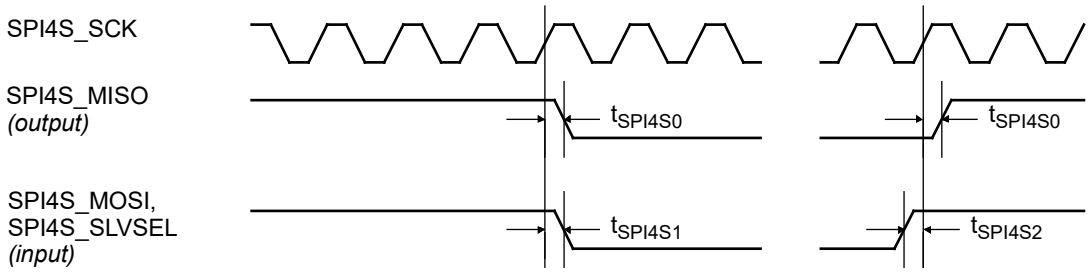

Figure 14. SPI interface timing waveforms

Table 27. SPI interface timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{SPI4S0_LVDS}	Clock to output delay	Rising SPI4S_CLK edge	0	30	ns
t_{SPI4S1_LVDS} 1)	Input to clock hold	Rising SPI4S_CLK edge	-	4	ns
t_{SPI4S2_LVDS} 1)	Input to clock setup	Rising SPI4S_CLK edge	-	4	ns

Note 1: Verified by static timing analysis, not tested in production.

2.13.10 SpaceWire LVDS interface timing

The timing waveforms are shown in figure 15, and the timing parameters are defined in table 28.

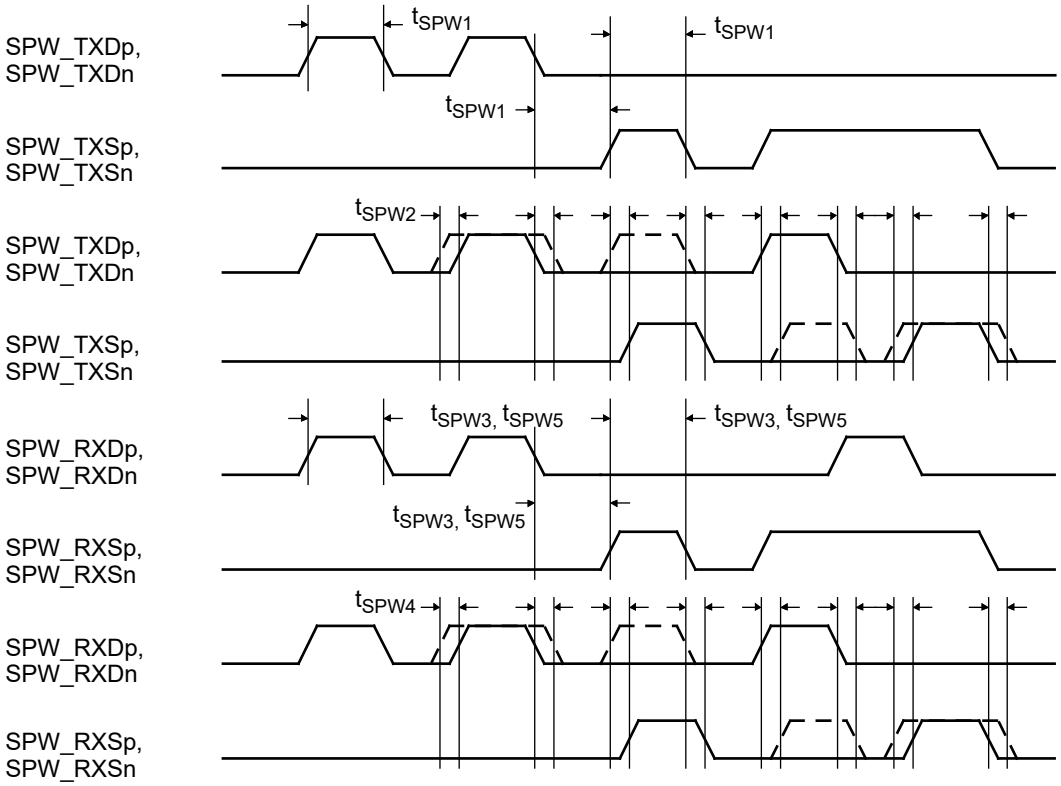

Figure 15. SpaceWire LVDS interface timing waveforms

Table 28. SpaceWire LVDS interface timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{SPW1_LVDS}	Output data bit period	-	5 [2)]	500 [1)]	ns
t_{SPW2_LVDS} [1)]	Data & strobe output skew & jitter	-	0	1.2	ns
t_{SPW3_LVDS} [1)]	Input data bit period	-	5	500	ns
t_{SPW4_LVDS} [1)]	Data & strobe input skew, jitter & hold	-	-	TBD	ns
t_{SPW5_LVDS} [1)]	Data & strobe edge separation	-	2.5	-	ns

Note 1: Verified by static timing analysis, not tested in production.

Note 2: Min values given here is from static timing analysis, in production test lowest value used is TBC ns.

2.13.11 CANFD interface timing

The timing waveforms and timing parameters are shown in figure 16 and are defined in table 29.

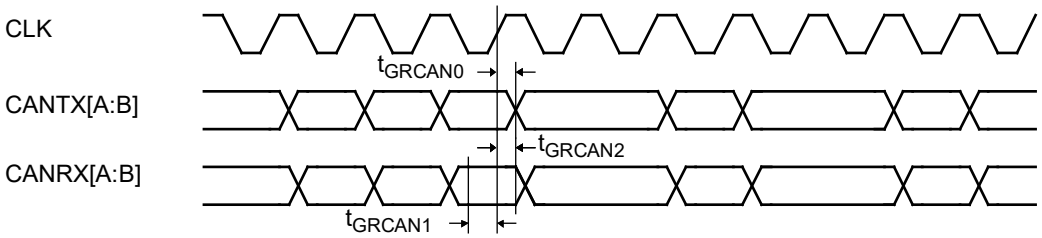

Figure 16. CANFD timing waveforms

Table 29. CANFD timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{GRCAN0}	clock to data output delay	rising *clk* edge	0	45	ns
t_{GRCAN1} [1)]	data input to clock setup	rising *clk* edge	-	4	ns
t_{GRCAN2} [1)]	data input from clock hold	rising *clk* edge	-	4	ns

Note 1: Verified by static timing analysis, not tested in production.

Note 2: The CAN inputs are re-synchronized to the internal system clock with a t_{CLK0} period. The signals do not have to meet any setup or hold requirements.

2.13.12 MIL-1553B interface timing

The timing waveforms and timing parameters are shown in figure 17 and are defined in table 30.

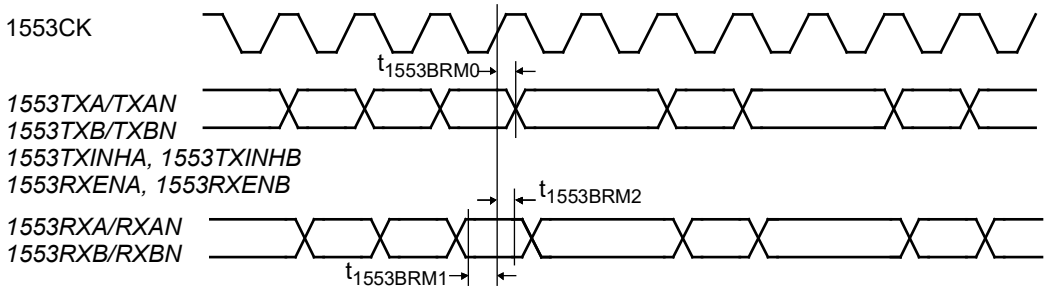

Figure 17. MIL-1553 timing waveforms

Table 30. MIL-1553 timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{1553BRM0}$	clock to data output delay	rising 1553CK edge	0	45	ns
$t_{1553BRM1}$ [1)]	data input to clock setup	rising 1553CK edge	-	4	ns
$t_{1553BRM2}$ [1)]	data input from clock hold	rising 1553CK edge	-	4	ns
$t_{1553BRM3}$	clock frequency	1553CK	20 [3)]		MHz

Note 1: Verified by static timing analysis, not tested in production.

Note 2: The 1553RXA, 1553RXAN, 1553RXB and 1553RXBN inputs are re-synchronized internally to 1553CK. The signals do not have to meet any setup or hold requirements.

Note 3: The GR1553CK clock domains are production tested at typical frequency of 20 MHz using a clock generated on external pins. For correct AC requirement on the MIL-1553B interface clock see MIL-STD-1553B / AS15531 standard document.

2.13.13 I2C-master

The timing waveforms and timing parameters are shown in figure 18 and are defined in table 31.

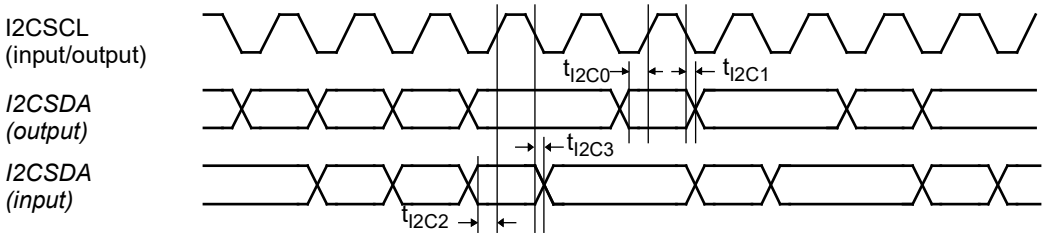

Figure 18. I2C-master timing waveforms

Table 31. I2C-master timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{I2C0}	data output valid before clock	rising I2CSCL edge	-	scaler [1)]	t_{CLK0} periods
t_{I2C1}	data output valid after clock	falling I2CSCL edge	scaler [1)]	-	t_{CLK0} periods
t_{I2C2} [5)]	data input setup to clock	rising I2CSCL edge	2 [2)]	-	t_{CLK0} periods
t_{I2C3} [5)]	data input hold from clock	falling I2CSCL edge	0 [2)]	-	t_{CLK0} periods

Note 1: The core's I2C bus functional timing depends on the IP-core's scaler value and the internal system clock t_{CLK0} period. When the scaler is set for the IP-core to operate in Fast- or Standard-Mode, the timing characteristics in the I2C-bus specification apply. The maximum t_{CLK0} period for proper operation is 50 ns.

Note 2: The I2CSCL and I2CSDA inputs are re-synchronized to the internal system clock with a t_{CLK0} period.

Note 3: I2CSCL and I2CSDA are open-drain outputs, driving a logical 0 level or tri-state.

Note 4: For correct operation, the signals should be pulled-up externally with 10 kΩ.

Note 5: Verified by static timing analysis, not tested in production.

2.13.14 Fault-tolerant 8-bit PROM/IO memory interface timing

The timing waveforms and timing parameters are shown in figures 19, and are defined in table 32.

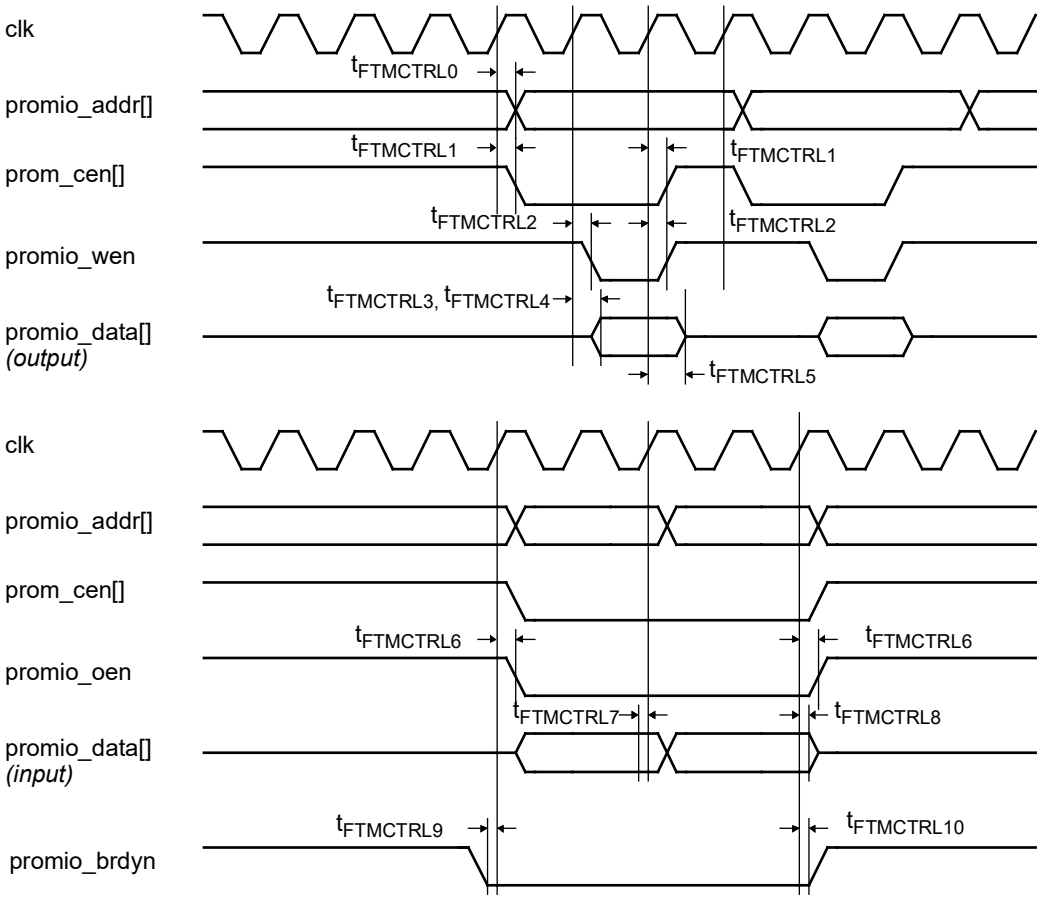

Figure 19. Timing waveforms - SRAM and PROM accesses

Table 32. PROM and I/O accesses timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{FTMCTRL0}$	address clock to output delay	rising clk edge	0	35	ns
$t_{FTMCTRL1}$	clock to output delay	rising clk edge	0	35	ns
$t_{FTMCTRL2}$	clock to output delay	rising clk edge	0	35	ns
$t_{FTMCTRL3}$	clock to data output delay	rising clk edge	0	35	ns
$t_{FTMCTRL4}$	clock to data non-tri-state delay	rising clk edge	0	35	ns
$t_{FTMCTRL5}$	clock to data tri-state delay	rising clk edge	5	35	ns
$t_{FTMCTRL6}$	clock to output delay	rising clk edge	0	35	ns
$t_{FTMCTRL7}$	data input to clock setup	rising clk edge	5	-	ns
$t_{FTMCTRL8}$	data input from clock hold	rising clk edge	-	-	ns
$t_{FTMCTRL9}$	input to clock setup	rising clk edge	5	-	ns
$t_{FTMCTRL10}$	input from clock hold	rising clk edge	-	-	ns

2.13.15 UART interface timing

The timing waveforms and timing parameters are shown in figure 20 and are defined in table 33.

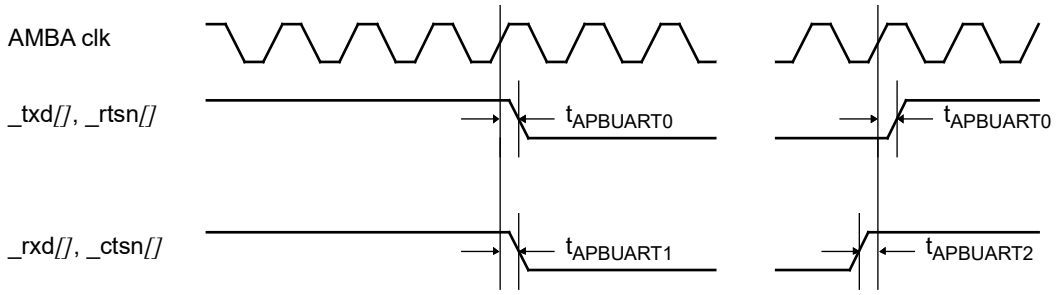

Figure 20. UART Timing waveforms

Table 33. UART timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{APBUART0}$	clock to output delay	rising clk edge	0	45	ns
$t_{APBUART1}$	input to clock hold	rising clk edge 2)	-	4 2)	ns
$t_{APBUART2}$	input to clock setup	rising clk edge 2)	-	4 2)	ns

Note 1: NA

Note 2: The _cstn and _rxd inputs are re-synchronized internally. These signals do not have to meet any setup or hold requirements.

2.13.16 DSU signals timing

The timing waveforms and timing parameters are shown in figure 21 and are defined in table 34.

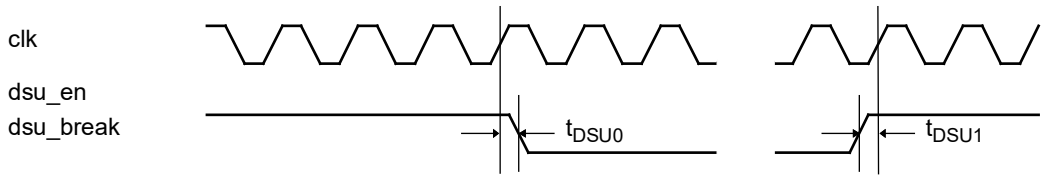

Figure 21. DSU timing waveforms

Table 34. DSU Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{DSU0}	input to clock hold	rising clk edge	- 1)	- 1)	ns
t_{DSU1}	input to clock setup	rising clk edge	- 1)	- 1)	ns

Note 1: The dsu_break and dsu_en signals are re-synchronized internally. These signals do not have to meet any setup or hold requirements. As the *dsu_en* signal controls clock gating for the Debug AHB bus the signal's value should be kept constant from power-up.

2.13.17 General purpose I/O timing

The timing waveforms are shown in figure 22, and the timing parameters are defined in table 35.

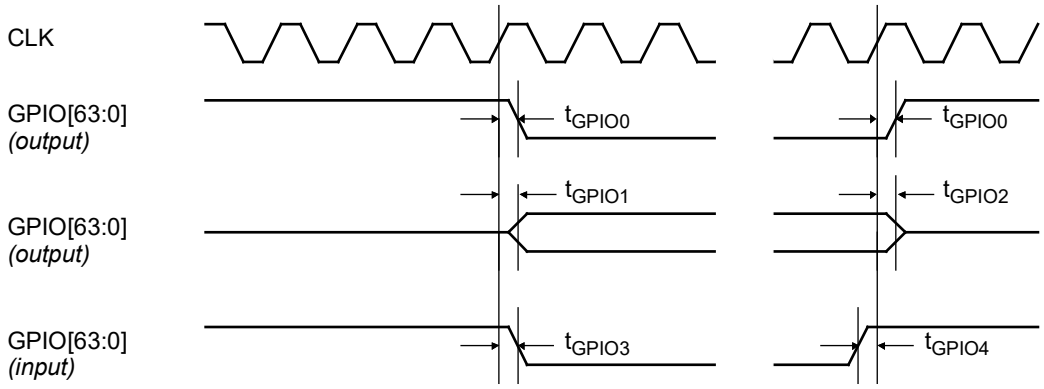

Figure 22. General purpose I/O timing waveforms

Table 35. General purpose I/O timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{GPIO0}	Clock to output delay	Rising CLK edge	0	45	ns
t_{GPIO1}	Clock to non-tri-state delay	Rising CLK edge	0	45	ns
t_{GPIO2}	Clock to tri-state delay	Rising CLK edge	0	45	ns
t_{GPIO3}	Input to clock hold	Rising CLK edge [1)]	-	-	ns
t_{GPIO4}	Input to clock setup	Rising CLK edge [1)]	-	-	ns
Note 1:	The GPIO[...] inputs are re-synchronized to the internal system clock				
Note 2:	NA				

2.13.18 NVRAM 16-bit memory interface timing

The timing waveforms and timing parameters are shown in figures 23, and are defined in table 37.

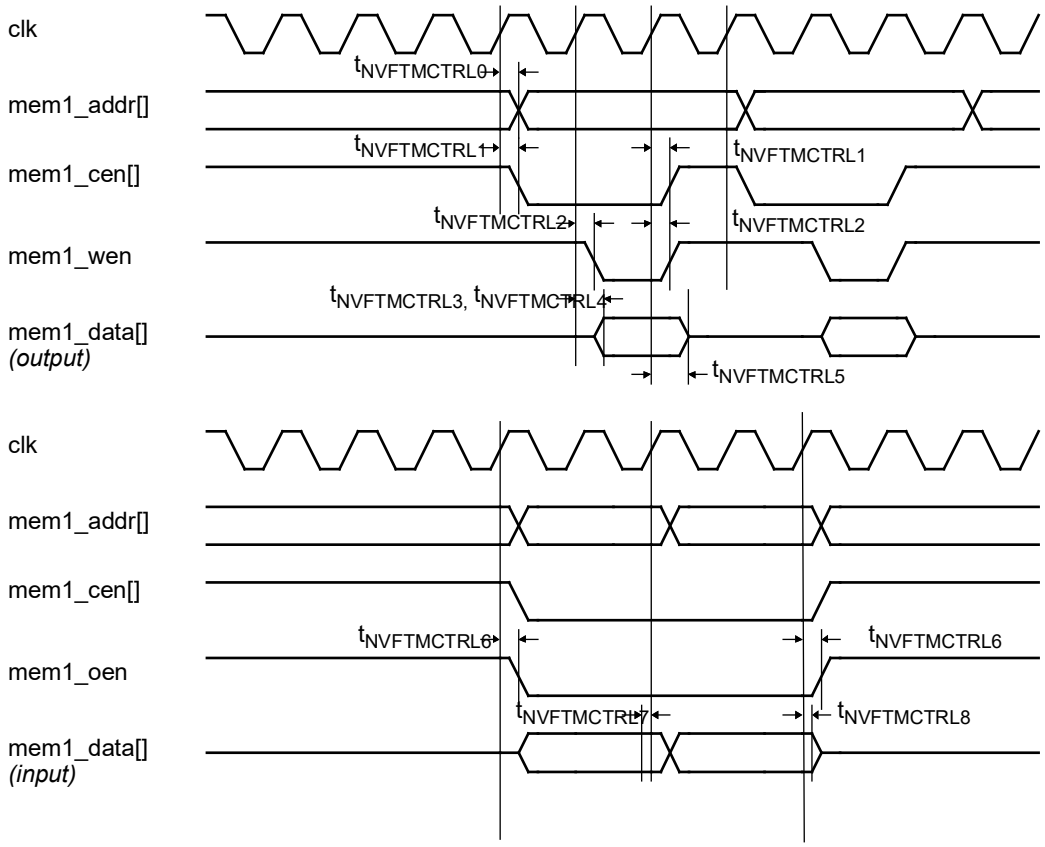

Figure 23. Timing waveforms - SRAM and PROM accesses

Table 36. NVRAM accesses timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{NVFTMCTRL0}$	address clock to output delay	rising clk edge	0	35	ns
$t_{NVFTMCTRL1}$	clock to output delay	rising clk edge	0	35	ns
$t_{NVFTMCTRL2}$	clock to output delay	rising clk edge	0	35	ns
$t_{NVFTMCTRL3}$	clock to data output delay	rising clk edge	0	35	ns
$t_{NVFTMCTRL4}$	clock to data non-tri-state delay	rising clk edge	0	35	ns
$t_{NVFTMCTRL5}$	clock to data tri-state delay	rising clk edge	5	35	ns
$t_{NVFTMCTRL6}$	clock to output delay	rising clk edge	0	35	ns
$t_{NVFTMCTRL7}$	data input to clock setup	rising clk edge	5	-	ns
$t_{NVFTMCTRL8}$	data input from clock hold	rising clk edge	-	-	ns
$t_{NVFTMCTRL9}$	input to clock setup	rising clk edge	5	-	ns
$t_{NVFTMCTRL10}$	input from clock hold	rising clk edge	-	-	ns

3 Mechanical description

3.1 Component and package

The GR716B PBGA product is provided in a 400-pin PBGA package with lead-free balls (SAC305 material). The Moisture Sensitivity Level (MSL) of this package is 4 in accordance with J-STD-020.

3.2 Pin assignment

The pin assignment in table below shows the implementation characteristics of each signal indicating how each pin has been configured in terms of electrical levels, drive capability and internal pull-up or pull-down.

Power supply and ground for all I/O pins are V_{DD_IO} and GND, unless otherwise noted.

Table 37. Pin assignment

Name	I/O	Pin	Level	Drive [mA]	Pull [2)]	Active	Unused [16)]	Note
TESTEN	in	B8	[15)]		Down	High	GND	Test mode enable. Pin shall always be connected to ground.
RESET_OUT_N	out	E1	[6)]	2 [6)]	Down [6)]	Low	Open	Buffered copy of the internal system reset.
RESET_IN_N	in [1)]	F1	[14)]		[14)]	Low	Pull to V_{DD_CORE}	Generates internal system reset, and activates RESET_OUT_N. 3.6V tolerant without ESD diode to any positive supply. **Supply:** V_{DD_CORE} vs GND
C_RST [3)]	-	G1	-			-	17)	Power-on reset timing. Connect to external capacitor.
VREFBUF	out	T1	1.9V			-	Pull to GND	Analog precision reference voltage. For electrical characteristics see 2.10. **Supply:** V_{DDA_REF} vs V_{SSA_REF}
VREF [4)]	-	U1	-			-	[17)]	Bandgap reference. Connect to external capacitor.
RREF [5)]	-	V1	-			-	[17)]	Bandgap reference. Connect to external resistor.
XO_OUT	out	Y14	CMOS	4		High	Open	Clock from crystal oscillator. Positive edge is performance characterized.
XO_X2	-	Y16	-			-	Pull to GND	Crystal oscillator. Connect to external crystal.
XO_X1	-	Y18	-			-	Pull to GND	Crystal oscillator. Connect to external crystal.
CLK	in [1)]	Y12	CMOS		Down	High	[17)]	System clock. It must always be applied.
SPWCLK	in [1)]	Y10	CMOS		Down	High	Pull to GND	SpaceWire and PLL clock
DSU_EN	in	D1	CMOS		Down	High	Pull to GND	DSU enable
DSU_BREAK	in	D2	CMOS		Down	High	Pull to GND	DSU break
DUART_RX	in [1)]	E3	CMOS		Down	High	Pull to GND	Debug UART data receive
DUART_TX	inout	D3	CMOS	4		High	Bootstrap [18)]	Debug UART data transmit
SPIM_SEL	inout	F3	CMOS	2		Low	Bootstrap [18)]	SPI Memory select
SPIM_SCK	inout	G3	CMOS	2		High	Bootstrap [18)]	SPI Memory data clock
SPIM_MOSI	inout	G4	CMOS	2		High	Bootstrap [18)]	SPI Memory master out / slave in
SPIM_MISO	in [1)]	G5	CMOS		Up	High	Pull to V_{DD_IO}	SPI Memory master in / slave out

Table 37. Pin assignment

Name	I/O	Pin	Level	Drive [mA]	Pull [2]	Active	Unused [16]	Note
LVDS_TX[0]p	out	T6	LVDS			High	Pull to GND [20]	LVDS transmitters, with **cold-spare capability**. See user manual section 2.5 [GR716B-UM] for functionality. **Supply:** V_{DD_LVDS} vs GND **Mapping for SpW:** LVDS_TX[0] → SPW_TXD0 LVDS_TX[1] → SPW_TXS0 LVDS_TX[2] → SPW_TXD1 LVDS_TX[3] → SPW_TXS1
LVDS_TX[0]n	out	R6	LVDS			Low	Pull to GND [20]	
LVDS_TX[1]p	out	P6	LVDS			High	Pull to GND [20]	
LVDS_TX[1]n	out	N6	LVDS			Low	Pull to GND [20]	
LVDS_TX[2]p	out	T8	LVDS			High	Pull to GND [20]	
LVDS_TX[2]n	out	R8	LVDS			Low	Pull to GND [20]	
LVDS_TX[3]p	out	P8	LVDS			High	Pull to GND [20]	
LVDS_TX[3]n	out	N8	LVDS			Low	Pull to GND [20]	
LVDS_TX[4]p	out	L17	LVDS			High	Pull to GND [20]	**Mapping for SpW:** LVDS_TX[4] → SPW_TXD1 LVDS_TX[5] → SPW_TXS1
LVDS_TX[4]n	out	L16	LVDS			Low	Pull to GND [20]	
LVDS_TX[5]p	out	L15	LVDS			High	Pull to GND [20]	
LVDS_TX[5]n	out	L14	LVDS			Low	Pull to GND [20]	
LVDS_RX[0]p	in	T10	LVDS			High	Pull to GND [19]	LVDS receivers with **extended common mode and cold-spare capabilities**. See user manual section 2.5 [GR716B-UM] for functionality. **Supply:** V_{DD_LVDS} vs GND **Mapping for SpW:** LVDS_RX[1] → SPW_RXD0 LVDS_RX[2] → SPW_RXS0 LVDS_RX[0] → SPW_RXD1 LVDS_RX[3] → SPW_RXS1
LVDS_RX[0]n	in	R10	LVDS			Low	Pull to GND [19]	
LVDS_RX[1]p	in	P10	LVDS			High	Pull to GND [19]	
LVDS_RX[1]n	in	N10	LVDS			Low	Pull to GND [19]	
LVDS_RX[2]p	in	T12	LVDS			High	Pull to GND [19]	
LVDS_RX[2]n	in	R12	LVDS			Low	Pull to GND [19]	
LVDS_RX[3]p	in	P12	LVDS			High	Pull to GND [19]	
LVDS_RX[3]n	in	N12	LVDS			Low	Pull to GND [19]	
GPIO[0]	inout	J19	CMOS	2	[8]	[8]	Bootstrap [18]	Schmitt trigger input selectable
GPIO[1]	inout	J18	CMOS	2	[8]	[8]	Bootstrap [18]	Schmitt trigger input selectable
GPIO[2]	inout	H20	CMOS	2	[8]	[8]	[13]	Schmitt trigger input selectable
GPIO[3]	inout	G20	CMOS	2	[8]	[8]	[13]	Schmitt trigger input selectable
GPIO[4]	inout	G19	CMOS	2	[8]	[8]	[13]	Schmitt trigger input selectable
GPIO[5]	inout	F20	CMOS	2	[8]	[8]	[13]	Schmitt trigger input selectable
GPIO[6]	inout	F19	CMOS	2	[8]	[8]	[13]	Schmitt trigger input selectable
GPIO[7]	inout	F18	CMOS	2	[8]	[8]	[13]	Schmitt trigger input selectable
GPIO[8]	inout	E20	CMOS	2	[8]	[8]	[13]	Schmitt trigger input selectable
GPIO[9]	inout	D20	CMOS	2	[8]	[8]	[13]	Schmitt trigger input selectable
GPIO[10]	inout	D19	CMOS	2	[8]	[8]	[13]	Schmitt trigger input selectable
GPIO[11]	inout	D18	CMOS	2	[8]	[8]	[13]	Schmitt trigger input selectable
GPIO[12]	inout	C20	CMOS	2	[8]	[8]	[13]	Schmitt trigger input selectable
GPIO[13]	inout	C19	CMOS	2	[8]	[8]	[13]	Schmitt trigger input selectable
GPIO[14]	inout	B19	CMOS	2	[8]	[8]	[13]	Schmitt trigger input selectable
GPIO[15]	inout	A18	CMOS	2	[8]	[8]	Bootstrap [18]	Schmitt trigger input selectable
GPIO[16]	inout	A17	CMOS	2	[8]	[8]	[13]	Schmitt trigger input selectable
GPIO[17]	inout	B17	CMOS	2	[8]	[8]	Bootstrap [18]	Schmitt trigger input selectable
GPIO[18]	inout	A16	CMOS	2	[8]	[8]	Bootstrap [18]	Schmitt trigger input selectable
GPIO[19]	inout	B16	CMOS	2	[8]	[8]	[13]	Schmitt trigger input selectable
GPIO[20]	inout	C16	CMOS	2	[8]	[8]	[13]	Schmitt trigger input selectable
GPIO[21]	inout	A15	CMOS	2	[8]	[8]	[13]	Schmitt trigger input selectable

Table 37. Pin assignment

Name	I/O	Pin	Level	Drive [mA]	Pull [2)]	Active	Unused [16)]	Note
GPIO[22]	inout	A14	CMOS	2	8)	8)	13)	Schmitt trigger input selectable
GPIO[23]	inout	B14	CMOS	2	8)	8)	13)	Schmitt trigger input selectable
GPIO[24]	inout	C14	CMOS	2	8)	8)	13)	Schmitt trigger input selectable
GPIO[25]	inout	A13	CMOS	2	8)	8)	13)	Schmitt trigger input selectable
GPIO[26]	inout	B13	CMOS	2	8)	8)	13)	Schmitt trigger input selectable
GPIO[27]	inout	C13	CMOS	2	8)	8)	13)	Schmitt trigger input selectable
GPIO[28]	inout	A12	CMOS	2	8)	8)	13)	Schmitt trigger input selectable
GPIO[29]	inout	A11	CMOS	2	8)	8)	13)	Schmitt trigger input selectable
GPIO[30]	inout	B11	CMOS	2	8)	8)	13)	Schmitt trigger input selectable
GPIO[31]	inout	A10	CMOS	2	8)	8)	13)	Schmitt trigger input selectable
GPIO[32]	inout	B10	CMOS	2	8)	8)	13)	Schmitt trigger input selectable
GPIO[33]	inout	C10	CMOS	2	8)	8)	13)	Schmitt trigger input selectable
GPIO[34]	inout	A9	CMOS	2	8)	8)	13)	Schmitt trigger input selectable
GPIO[35]	inout	A8	CMOS	2	8)	8)	13)	Schmitt trigger input selectable
GPIO[36]	inout	C8	CMOS	2	8)	8)	13)	Schmitt trigger input selectable
GPIO[37]	inout	K1	CMOS[7)]	2 [7)]	8)	8)	13)	General purpose IO with analog **ADC and ACOMP input capabilities**, with ground ref VSSA_REF. See user manual section 2.5 [GR716B-UM] for functionality. **Supply:** V_{DDA_ADC} vs V_{SSA_ADC}
GPIO[38]	inout	L2	CMOS [7)]	2 [7)]	8)	8)	13)	
GPIO[39]	inout	M1	CMOS [7)]	2 [7)]	8)	8)	13)	
GPIO[40]	inout	M3	CMOS [7)]	2 [7)]	8)	8)	13)	
GPIO[41]	inout	N2	CMOS [7)]	2 [7)]	8)	8)	13)	
GPIO[42]	inout	P1	CMOS [7)]	2 [7)]	8)	8)	13)	
GPIO[43]	inout	P3	CMOS [7)]	2 [7)]	8)	8)	13)	
GPIO[44]	inout	R2	CMOS[7)]	2 [7)]	8)	8)	13)	
GPIO[45]	inout	Y4	CMOS [7)]	2 [7)]	8)	8)	13)	General purpose IO with analog **DAC output and ACOMP input capabilities**. See user manual section 2.5 [GR716B-UM] for functionality. **Supply:** V_{DDA_DAC} vs V_{SSA_DAC}
GPIO[46]	inout	W5	CMOS [7)]	2 [7)]	8)	8)	13)	
GPIO[47]	inout	Y6	CMOS [7)]	2 [7)]	8)	8)	13)	
GPIO[48]	inout	W7	CMOS [7)]	2 [7)]	8)	8)	13)	
GPIO[49]	inout	T16	CMOS	2	8)	8)	13)	Schmitt trigger input selectable
GPIO[50]	inout	P16	CMOS	2	8)	8)	13)	Schmitt trigger input selectable
GPIO[51]	inout	U20	CMOS [7)]	2 [7)]	8)	8)	13)	General purpose IO with analog **ADC and ACOMP input capabilities**, with ground ref GND_ADC3. See user manual section 2.5 [GR716B-UM] for functionality. **Supply:** V_{DD_IO} vs GND
GPIO[52]	inout	U18	CMOS [7)]	2 [7)]	8)	8)	13)	
GPIO[53]	inout	T19	CMOS [7)]	2 [7)]	8)	8)	13)	
GPIO[54]	inout	R20	CMOS [7)]	2 [7)]	8)	8)	13)	
GPIO[55]	inout	R18	CMOS [7)]	2 [7)]	8)	8)	13)	
GPIO[56]	inout	P19	CMOS [7)]	2 [7)]	8)	8)	13)	
GPIO[57]	inout	N20	CMOS [7)]	2 [7)]	8)	8)	13)	
GPIO[58]	inout	N18	CMOS [7)]	2 [7)]	8)	8)	13)	
GPIO[59]	inout	L19	CMOS	2	8)	8)	13)	GPIO [59] to [62] cannot be used along with LVDS_TX[4] and LVDS_TX[5]. See user manual section 2.5 [GR716B-UM] for functionality.
GPIO[60]	inout	K20	CMOS	2	8)	8)	13)	
GPIO[61]	inout	K19	CMOS	2	8)	8)	13)	
GPIO[62]	inout	K18	CMOS	2	8)	8)	Bootstrap [18)]	

Table 37. Pin assignment

Name	I/O	Pin	Level	Drive [mA]	Pull [2)]	Active	Unused [16)]	Note
GPIO[63]	inout	J20	CMOS	2	[8)]	[8)]	Bootstrap [18)]	Schmitt trigger input selectable
MEM1_ADDR[0]	out	D11	CMOS	2		High	Open	In 8-bit mode, use MEM1_ADDR[22:0] to interface with PROM/SRAM devices Do not use MEM1_ADDR[0] when interfacing with 16-bit external memory
MEM1_ADDR[1]	out	D10	CMOS	2		High		In 16-bit mode, use MEM1_ADDR[22:1] as address bus
MEM1_ADDR[2]	out	D9	CMOS	2		High		
MEM1_ADDR[3]	out	D8	CMOS	2		High		
MEM1_ADDR[4]	out	D7	CMOS	2		High		
MEM1_ADDR[5]	out	E8	CMOS	2		High		
MEM1_ADDR[6]	out	E7	CMOS	2		High		
MEM1_ADDR[7]	out	F8	CMOS	2		High		
MEM1_ADDR[8]	out	F7	CMOS	2		High		
MEM1_ADDR[9]	out	F6	CMOS	2		High		
MEM1_ADDR[10]	out	G10	CMOS	2		High		
MEM1_ADDR[11]	out	G9	CMOS	2		High		
MEM1_ADDR[12]	out	G8	CMOS	2		High		
MEM1_ADDR[13]	out	G7	CMOS	2		High		
MEM1_ADDR[14]	out	G6	CMOS	2		High		
MEM1_ADDR[15]	out	H8	CMOS	2		High		
MEM1_ADDR[16]	out	H7	CMOS	2		High		
MEM1_ADDR[17]	out	H6	CMOS	2		High		
MEM1_ADDR[18]	out	J7	CMOS	2		High		
MEM1_ADDR[19]	out	J6	CMOS	2		High		
MEM1_ADDR[20]	out	K7	CMOS	2		High		
MEM1_ADDR[21]	out	K6	CMOS	2		High		
MEM1_ADDR[22]	out	L7	CMOS	2		High		
MEM1_CSN[0]	out	E13	CMOS	2		Low		
MEM1_CSN[1]	out	F13	CMOS	2		Low		
MEM1_CSN[2]	out	E11	CMOS	2		Low		
MEM1_CSN[3]	out	F11	CMOS	2		Low		
MEM1_CSN[4]	out	E10	CMOS	2		Low		
MEM1_CSN[5]	out	F10	CMOS	2		Low		
MEM1_OEN	out	D13	CMOS	2		Low		
MEM1_WEN	out	D12	CMOS	2		Low		
MEM1_RSTN	out	L6	CMOS	2		Low	Open	

Table 37. Pin assignment

Name	I/O	Pin	Level	Drive [mA]	Pull [2)]	Active	Unused [16)]	Note
MEM1_DATA[0]	inout	H17	CMOS	2		High		In 16-bit mode, MEM1_-DATA[15:0] should be used as data bus
MEM1_DATA[1]	inout	H14	CMOS	2		High		
MEM1_DATA[2]	inout	G17	CMOS	2		High		
MEM1_DATA[3]	inout	G16	CMOS	2		High		
MEM1_DATA[4]	inout	G15	CMOS	2		High		
MEM1_DATA[5]	inout	G14	CMOS	2		High		
MEM1_DATA[6]	inout	F17	CMOS	2		High		
MEM1_DATA[7]	inout	F16	CMOS	2		High		
MEM1_DATA[8]	inout	F14	CMOS	2		High		In 8-bit mode, the PROM/SRAM devices should be connected to the MSB byte of the data bus (MEM1_DATA[15:8])
MEM1_DATA[9]	inout	E17	CMOS	2		High		
MEM1_DATA[10]	inout	E16	CMOS	2		High		
MEM1_DATA[11]	inout	E14	CMOS	2		High		
MEM1_DATA[12]	inout	D17	CMOS	2		High		
MEM1_DATA[13]	inout	D16	CMOS	2		High		
MEM1_DATA[14]	inout	D15	CMOS	2		High		
MEM1_DATA[15]	inout	D14	CMOS	2		High		
MEM1_CONFIG[0]	in	A7	CMOS	2	UP	Low	Bootstrap [18)]	Pull resistance shall be 0 to 3 kohm
MEM1_CONFIG[1]	in	B7	CMOS	2	UP	Low	Bootstrap [18)]	Pull resistance shall be 0 to 3 kohm
MEM1_CONFIG[2]	in	C7	CMOS	2	UP	Low	Bootstrap [18)]	Pull resistance shall be 0 to 3 kohm
RESERVED		G11, G12, G13, H13, J14, J15, J16, J17						Reserved pins for future use. These pins have no internal connection and should not be left floating on the PCB. E.g., connect them to ground, use a pull-down resistor, or drive them with any signal from the PCB
VDD_CORE	-	A1, A2, A4, B1, B3, B6, C2, C11, C17, F2, G18, H9, H12, J9, J12, K9, K12, K14, L9, L12, M5, M7, M9, M12, M14, M16, N13, N15, P5, P14, R13, R15, T5, U7, U9, U11, U16					[9)]	Core 1.8V supply [9) 10)]

Table 37. Pin assignment

Name	I/O	Pin	Level	Drive [mA]	Pull [2]	Active	Unused [16]	Note
VDD_IO	-	C3, C6, C9, C12, C15, C18, E18, F9, F12, F15, H2, H5, H15, H18, K5, K16, L18, P17, T17, V17, W10, W12, W14					[17]	I/O 3.3V supply [10]
VDD_LVDS	-	P7, P9, P11, T7, T9, T11					[17]	LVDS I/O 3.3V supply [10]
VDD_LDO	-	A3, A5, B2, B4, B5					[9]	LDO 3.3V supply [9] [10]
GND	-	A6, A19, A20, B9, B12, B15, B18, B20, C1, C4, C5, E2, E9, E12, E15, E19, G2, H1, H3, H4, H10, H11, H16, H19, J5, K15, K17, L5, L20, M17, M19, N9, N11, P13, P15, R9, R11, T13, T14, T15, U5, U8, U10, U12, V9, V10, V11, V12, V15, V16, V19, W9, W11, W13, W15, W16, W17, W18, W19, W20, Y9, Y11, Y13, Y15, Y17, Y19, Y20, D4, D5, D6, E4, E5, E6, F4, F5, J8, J10, J11, J13, K8, K10, K11, K13, L8, L10, L11, L13, M6, M8, M10, M11, M13, M15, N5, N7, N14, N16, R5, R7, R14, R16, U6, U15					[17]	Digital ground [10]
VDDA_ADC	-	J4, U4					[17]	ADC 3.3V analog supply [10] [12]
VSSA_ADC	-	J3, K4, T4, U3					[17]	ADC analog ground [10] [12]

Table 37. Pin assignment

Name	I/O	Pin	Level	Drive [mA]	Pull [2)]	Active	Unused [16)]	Note
VDDA_REF	-	U2, W2					17)	REF 3.3V analog supply 10) 12)
VSSA_REF	-	J1, J2, K2, K3, L1, L3, L4, M2, M4, N1, N3, N4, P2, P4, R1, R3, R4, T2, T3, V2, W1, Y1, Y2					17)	REF analog ground 10) 12)
VDDA_DAC	-	W3, W4, W6, W8					17)	DAC 3.3V analog supply 10) 12)
VSSA_DAC	-	V3, V4, V5, V6, V7, V8, Y3, Y5, Y7, Y8					17)	DAC analog ground 10) 12)
VDDA_PLL	-	U14, V13					17)	PLL 1.8V analog supply 11)
VSSA_PLL	-	U13, V14					17)	PLL analog ground 11)
GND_ADC3	-	M18, M20, N17, N19, P18, P20, R17, R19, T18, T20, U17, U19, V18, V20					17)	ADC3 analog ground reference. GND_ADC3 shall be connected to the same ground plane as VSSA_REF on PCB, to maintain full functionality and performance of ADC3.

Note 1: Schmitt trigger input.

Note 2: Internal pull up/down resistor is 30kΩ unless otherwise stated, which can be regarded a weak pull value but should be able to keep the internal chip signal at safe level in case of pin open-circuit failure, since no external PCB wire then is present to pick up disturbances. If a pin will be unused, it is recommended to connected a pull resistor on PCB with lower value to ensure safe level against disturbances.

Note 3: Connect only to ground via external capacitor. It is not recommended to leave the C_{RST} pin unconnected, due to disturbance risk from other PCB circuitry, which could generate false reset. For functional capacitance values see section 2.11.

Note 4: Connect only to ground via 4.7nF decoupling capacitor.

Note 5: Connect only to ground via resistance of 5.11kΩ.

Note 6: RESET_OUT_N output drive capability is 2mA CMOS at high level and internal passive pull-down of 10kΩ at low level. It is valid also during power ramp up and down due to the passive pull-down resistor. External leakage or disturbance from PCB circuitry, pulling this node up, is recommended to not exceed 10uA to ensure a safe low level. Refer user manual section 8 [GR716B-UM] for more information regarding reset.

Note 7: Applies only for digital CMOS functionality.

Note 8: Parameter is programmable when digital functionality is selected for pin. Pull up/down resistor value is 50kΩ.

Note 9: In single supply mode, V_{DD_LDO} is recommended to be connected to same 3.3V supply as V_{DD_IO} (for simultaneous ramp up/down), and no external 1.8V supply shall be connected to V_{DD_CORE}. In single supply mode, the maximum decoupling capacitance on V_{DD_CORE} must not be more than 400 uF (well damped).

In dual supply mode, V_{DD_LDO} should be connected to V_{DD_CORE}, and external 1.8V supply connected to V_{DD_CORE}.

Note 10: External decoupling should be added in all supply modes and as close as possible to the supply pins. Typically add a 10nF ceramic capacitor per supply pin pair (e.g. X7R), and distributed across the PCB at least two 100uF well damped capacitors (or add 0.1Ω pulse-withstand rated resistor in series with each ceramic 100uF capacitor).

Note 11: The PLL supply pin pair, V_{DDA_PLL} and V_{SSA_PLL}, is supplied from internal LDO. External decoupling should be a ceramic capacitor of about 2uF (e.g. 2.2uF, X7R). The V_{DDA_PLL} pin must not be connected to anything else on PCB.

Table 37. Pin assignment

Name	I/O	Pin	Level	Drive [mA]	Pull [2)]	Active	Unused [16)]	Note
Note 12:	It is recommended to use separate power supplies for analog supply or to insert local LP filters. For example, use one LP filter with 1Ω resistor (pulse-withstand rated) and 10uF (typically X7R) that supplies all three analog domains (V_{DDA_ADC}, V_{DDA_DAC} and V_{DDA_REF}). Also decouple each V_{DDA} pin with 10nF (typically X7R). V_{SSA_ADC} and GND_ADC3 must be locally connected to same PCB ground as V_{SSA_REF}, to maintain ADC functionality and performance.							
Note 13:	Unused GPIO pin should have a pull-down of 10kΩ to ground, and it can then be configured to arbitrary mode (input, output, disable, etc). Alternatively, the pin can be left open but it should then be configured to digital output at all times.							
Note 14:	Internal pull resistor of 100kΩ to V_{DD_CORE}. See section 2.11 for further electrical characteristics. Refer to user manual section 8 [GR716B-UM] for more information regarding reset.							
Note 15:	TESTEN input shall always be low-impedance grounded, also during supply voltage ramp up and down.							
Note 16:	This column specifies termination for unused pins. The termination resistance is recommended to be 10kΩ unless otherwise noted. The pin state is assumed to be stable immediately after power-on or reset of the device.							
Note 17:	Pin should always be connected according to table in 2.2.							
Note 18:	Bootstrap pins should always be strapped to V_{DD_IO} or GND via 10 kΩ, unless otherwise noted, depending on selected boot mode. See user manual section 3.1 [GR716B-UM] for more information.							
Note 19:	When an LVDS receiver is enabled, it will not be damaged by inputs left unconnected, but it should not have fail-safe enabled. Random data to the core logic could be generated by disturbance if differential input voltage happens to be close to zero. To avoid these issues it is recommended that an unused or unconnected receiver is disabled, which also will save power consumption.							
Note 20:	LVDS transmitters should be disabled when not used.							

3.3 Mechanical package drawings

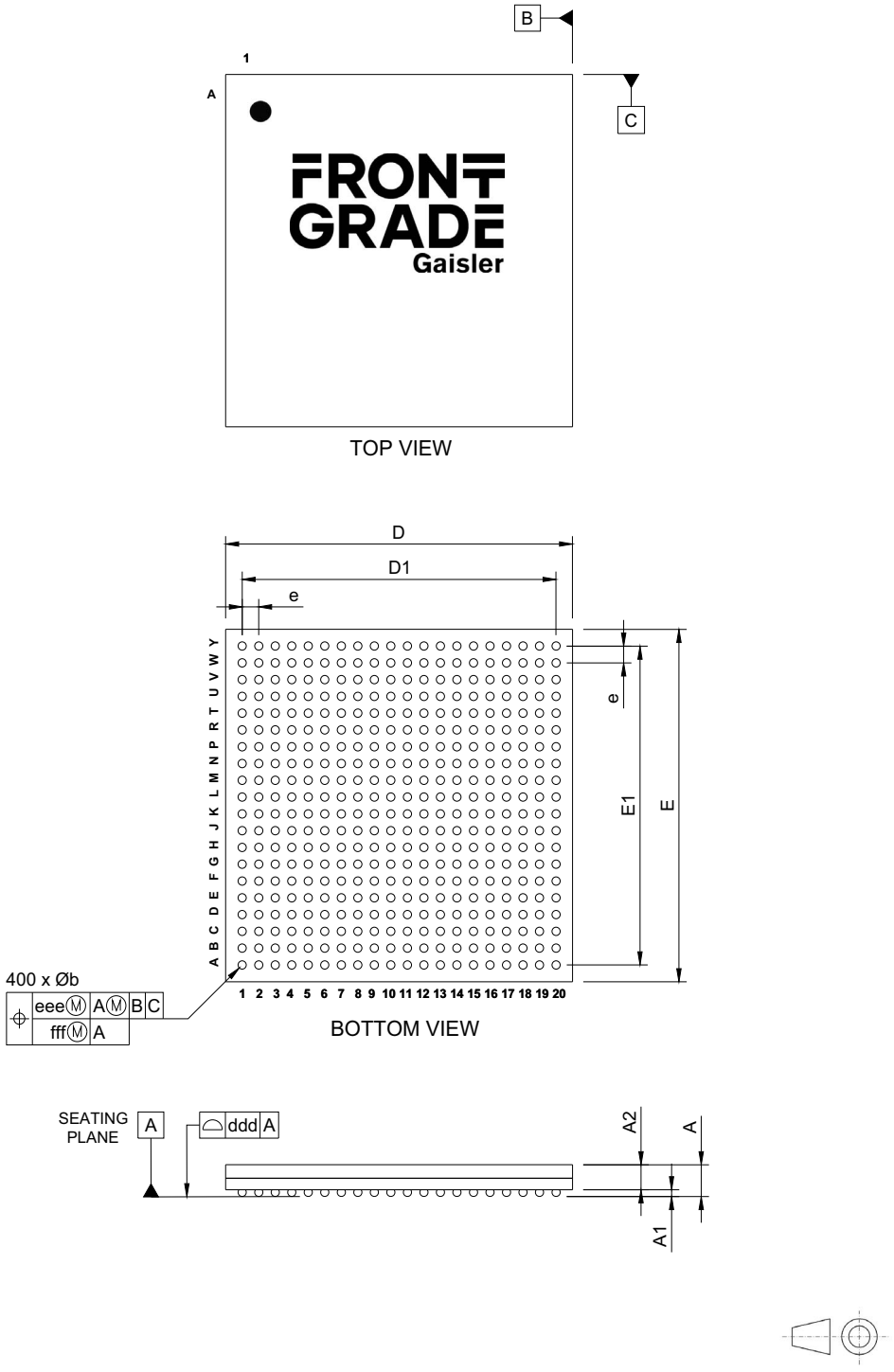

Figure 24. Package top and bottom view

Table 38. Package dimensions

SYMBOL	MIN[mm]	TYP [mm]	Max [mm]	Notes
A	1.74	1.89	2.04	A= A1+A2
A1	0.35	0.4	0.45	
A2	1.39	1.49	1.59	
D/E	20.9	21	21.1	
D1/E1		19		
b		0.5		
e		1		
ddd		0.2		
eee			0.15	
fff			0.08	

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