

## GR-AVANTX-MINI board user's manual

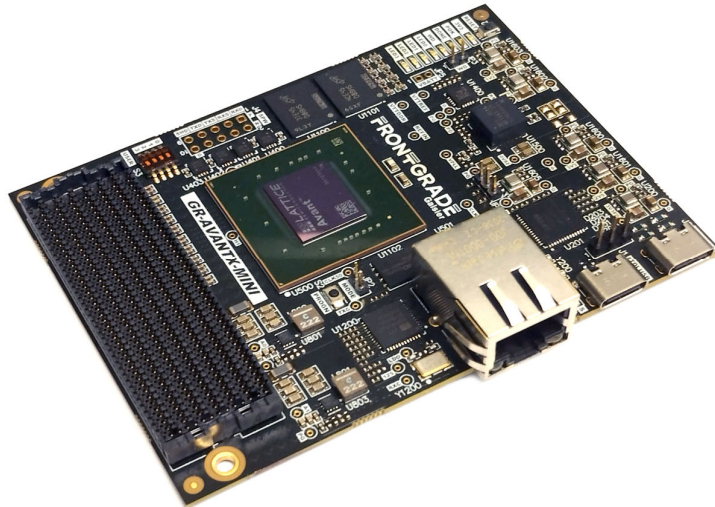
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User manual

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## 1 INTRODUCTION

### 1.1 Purpose and scope of the document

This document provides a user's manual and interface document for the GR-AVANTX-MINI FPGA board.

The GR-AVANTX-MINI board is a compact evaluation platform (7x9.5cm form factor) built around the Lattice Semiconductor Avant-X70 FPGA [RD2]. The board is designed with multiple electrical functions and interfaces which allows the user to interact with the FPGA and to develop designs based on the Frontgrade Gaisler's GRLIB IP library [RD3].

The board was designed by Frontgrade Gaisler AB, Gothenburg, Sweden, in collaboration with Pender Electronic Design, Zurich, Switzerland.

### 1.2 Handling precautions



**ATTENTION: OBSERVE PRECAUTIONS FOR  
HANDLING ELECTROSTATIC SENSITIVE DEVICES**

The board contains sensitive electronic components which can be damaged by ESD. When handling or installing the board, observe appropriate precautions and ESD safe practices.

When not in use, store the board in an electrostatic protective container or bag.

When configuring the jumpers on the board or connecting/disconnecting cables, ensure that the board is in an un-powered state.

When operating the board in a standalone configuration, the power supply should be current-limited to prevent damage to the board or power supply in the event of an overcurrent situation.

### 1.3 Reference documents

The following documents are referred as they contain relevant information:

[RD1] "GR-AVANTX-MINI," Pender Electronic Design, PED-00439-SCH, revision 1.1.

[RD2] "Avant-X – High-Speed Mid-Range FPGA," Lattice Semiconductor.

Available online at: <https://www.latticesemi.com/en/Products/FPGAandCPLD/Avant-X>

[RD3] "GRLIB IP library," Frontgrade Gaisler.

Available online at: <https://www.gaisler.com/grlib>

[RD4] "Lattice Avant Platform – Overview," Lattice Semiconductor.

Available online at: <https://www.latticesemi.com/en/Products/FPGAandCPLD/Avant-X>

[RD5] "GRMON4," Frontgrade Gaisler.

Available online at: <https://www.gaisler.com/products/grmon4>

[RD6] "Lattice Avant sysCLOCK PLL Design User Guide," Lattice Semiconductor.

Available online at: <https://www.latticesemi.com/en/Products/FPGAandCPLD/Avant-X>

[RD7] “Lattice Radiant Software,” Lattice Semiconductor.

Available online at: <https://www.latticesemi.com/radiant>

[RD8] “Lattice Avant sysCONFIG User Guide,” Lattice Semiconductor.

Available online at: <https://www.latticesemi.com/en/Products/FPGAandCPLD/Avant-X>

[RD9] “Lattice Avant Hardware Checklist,” Lattice Semiconductor.

Available online at: <https://www.latticesemi.com/en/Products/FPGAandCPLD/Avant-X>

[RD10] “DDR Memory PHY Module,” Lattice Semiconductor.

Available online at:

<https://www.latticesemi.com/en/Products/DesignSoftwareAndIP/IntellectualProperty/IPCore/IPCores05/MemoryController>

[RD11] “DDR Memory Controller IP Core,” Lattice Semiconductor.

Available online at:

<https://www.latticesemi.com/en/Products/DesignSoftwareAndIP/IntellectualProperty/IPCore/IPCores05/MemoryController>

## 2 ABBREVIATIONS

CRAM	Configuration Random-Access Memory
DDR4	Double Data Rate 4 SDRAM
DDRPHY	DDR Physical Layer
DQ	Data bit
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	Electrostatic Discharge
FCBGA	Fine-pitch Column Ball Grid Array
FinFET	Fin Field-Effect Transistor
FMC	FPGA Mezzanine Card
FPGA	Field-Programmable Gate Array
FTDI	Future Technology Devices International
GA	Geographic Address
HPC	High Pin Count
IP	Intellectual Property
JTAG	Joint Test Action Group
LDO	Low-Dropout
LVDS	Low-Voltage Differential Signaling
LVTTL	Low-Voltage Transistor-Transistor Logic
M2C	Mezzanine to Carrier
MDIO	Management Data Input/Output
MDM	Multi-pin D-type Miniature
MMD	MDIO Management Device
PCB	Printed Circuit Board
PD	USB Power Delivery standard
PHY	Physical Layer
PLL	Phase-Locked Loop
RGMII	Reduced Gigabit Media Independent Interface
SDRAM	Synchronous Dynamic Random-Access Memory
SerDes	Serializer/Deserializer
SPI	Serial Peripheral Interface
SRAM	Static Random-Access Memory
TCK	Test Clock
TDI	Test Data In
TDO	Test Data Out
TMS	Test Mode Select
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
USB-C	USB Type-C
VADJ	Adjustable I/O Voltage
VBUS	Voltage Bus

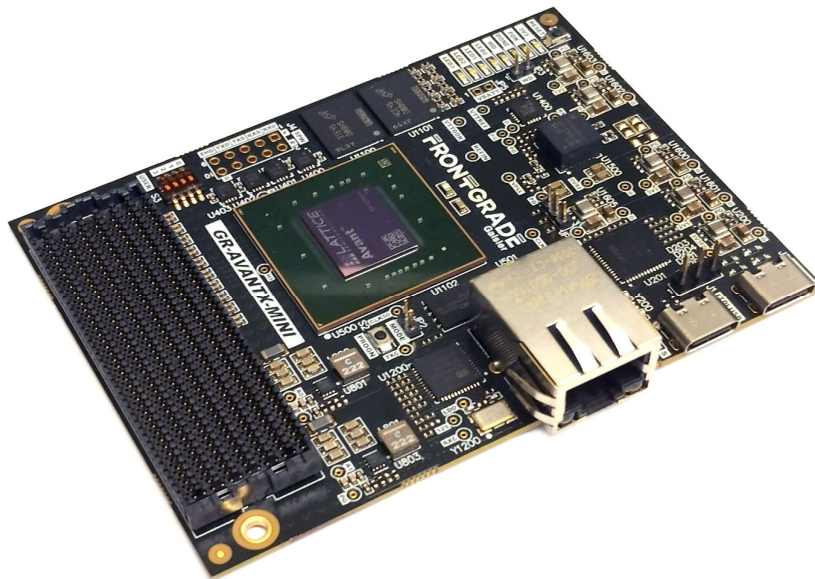
The list is not exhaustive and covers only abbreviations used in the text, not in the tables.

### 3 BOARD OVERVIEW

The GR-AVANTX-MINI is a compact evaluation platform (7x9.5cm form factor) built around the Lattice Avant-X70 FPGA (LAV-AT-X70-3LFG676C) [RD2]. The board is designed with multiple electrical functions and interfaces which allows the user to interact with the FPGA and to develop designs based on the Frontgrade Gaisler's GRLIB IP library [RD3]. Figure 1 shows a picture of the board.

The board contains the following main components:

- Lattice Avant-X70 FPGA in 676-ball FCBGA package (LAV-AT-X70-3LFG676C).
- 2x USB-C connectors for power supply, FPGA programming, and UART/JTAG debugging (via FTDI FT4232H).
- 4GB DDR4 SDRAM (2x Micron MT40A2G8AG, 16-bit bus).
- 2x 512Mb SPI Flash (Macronix MX25L51245G): one for FPGA configuration, one for user data.
- 1x Gigabit Ethernet with RJ45 connector (Microchip KSZ9031RNX PHY).
- FMC+ HPC connector (560-pin, ASP-184329-01) with 67x differential signals (LVDS, 134x single-ended), 8x SerDes lanes (2x quads), and on-board VADJ configuration (1.2V, 1.5V, 1.8V).
- 50MHz and 100MHz LVTTTL input clocks. 100MHz and 156.25MHz LVDS reference clocks.
- On-board power regulation from USB-C input (+5V).



*Figure 1. View of the GR-AVANTX-MINI board.*

## 4 BOARD DESIGN

This section describes the board design in detail. The interfaces and electrical functions are described subsection by subsection.

» This design is an evaluation platform and is not intended for use in safety-critical applications.

### 4.1 Block diagram and main interfaces

The GR-AVANTX-MINI board is built around a single Lattice Avant-X70 FPGA. Figure 2 shows the top-level block diagram of the board. Figure 3 highlights the user interfaces to the board. Appendix A contains a more detailed view of the assembly of the board. The schematic file [RD1] is provided only upon the procurement of the board.

The communication with the Avant-X70 FPGA is possible through multiple interfaces:

- **USB-C:** the USB-C link is connected to an FTDI chip that converts the USB-data into three serial interfaces (1x JTAG and 2x UART) connected to the FPGA. The USB-C interface for communication is connected to connector J2.
- **Ethernet:** an RGMII interface to the FPGA is provided through the RJ45 connector J3.
- **FMC+ HPC connector:** the usage of the FMC+ HPC connector (FMC1) is dependent on an external mezzanine board. In this design, the FMC+ HPC connector provides 67x LVDS pairs (or 134x single-ended signals), 8x SerDes pairs (2x quads), and adjustable VADJ (on-board).
- **SpaceWire:** a SpaceWire-capable 2x5 pin-header footprint is provided on the board (connector J4). The interface is fitted with LVDS buffers/repeaters but no connector (MDM-9).

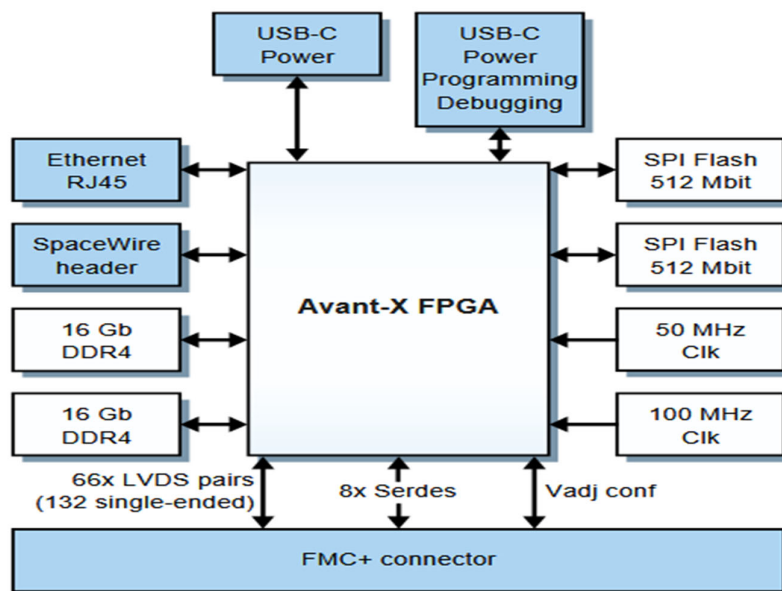


Figure 2. Block diagram of the GR-AVANTX-MINI board.

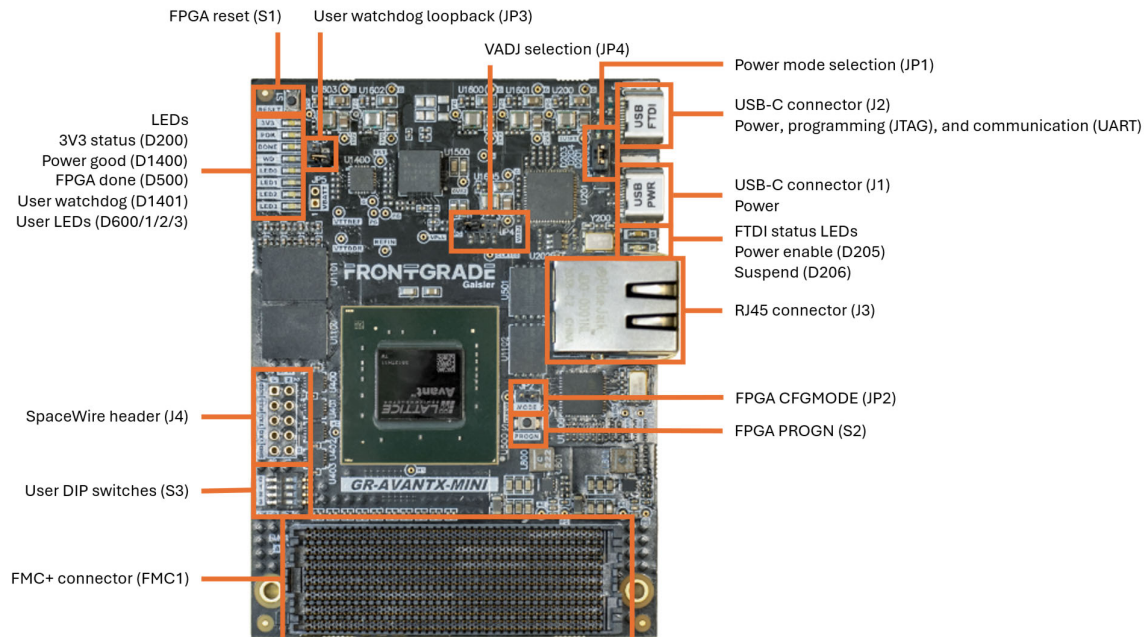


Figure 3. Top view of the GR-AVANTX-MINI board.

## 4.2 Power and reset

» The overall power requirement of the GR-AVANTX-MINI board is 15W. One should notice that, regardless of the power supply mode, the board shall be supplied with at least 3A/5V (15W).

The GR-AVANTX-MINI board can be powered in two different modes via the USB-C connectors J2 and J1. The 3-pin jumper JP1 allows the selection of the power mode.

USB-C connector J2 (JP1: 2-3) can be considered as the default power supply mode of the board, as this is also the connector used for JTAG and UART communication (via FTDI FT4232H).

Supplying the board via connector J2 and a standard USB-C source should be sufficient for a normal operation of the Avant-X70 FPGA. However, there may be a scenario in which the USB source connected to J2 (for communication) is not able to fulfil the power requirement of the board. In this case, an external power supply source can be connected to the USB-C connector J1 (JP1: 1-2). The input voltage range allowed is  $+5V \pm 5\%$ .

» The power supply source (for example a computer, charger, or docking station) shall have an USB-C connector that can deliver at least 3A/5V (15W). Observe that not all sources with USB-C sockets support that. Check the user manual/datasheet of the source before connecting it to the GR-AVANTX-MINI board.

All on-board power supplies are generated from the USB-C's VBUS bus (5V). Table 1 lists all the on-board power supply rails. The 3V3 LED (D200) lights up green once the  $+3V3FT$  supply is generated. The Power Good LED (D1400) lights up green when the power-up sequence is completed and the Reset signal is de-asserted (active low).

*Table 1. Power supply rails of the GR-AVANTX-MINI board.*

Rail	Voltage	Regulator	Load
VBUS_5V	3-17V input	J2 or J1	Board input rail
+3V3FT	3.3V	U200	FTDI FT4232H
+0V82	0.82V	U1500	FPGA core
+3V3	3.3 V	U1600	FPGA I/O, FTDI, Ethernet PHY, SPI Flash
+2V5	2.5V	U1601	FPGA I/O, DDR4 VPP
+1V8	1.8V	U1602	FPGA VCCAUX, FPGA I/O banks
+1V2	1.2V	U1603	FPGA DDR banks, DDR4 VDD/VDDQ
VADJ	1.2/1.5/1.8V	U1605	FMC VADJ (JP4 selectable)
VTTDDR	0.6V	U1604	DDR4 termination
VTTREF	0.6V	U1604	DDR4 VTTREF

The power sequencer on the board (U1400) manages the power-up and power-down sequence of all on-board voltage rails. The sequencer monitors the power good signals from the different regulators on the board and asserts the enable signal of the next rail in sequence once the previous one has settled.

The Reset push button (S1) asserts the Reset signal (active low).

A signal named WDOGN (active low), which is intended to be a Watchdog output from the FPGA design, is connected to the power sequencer. Jumper JP3 can disconnect the signal if not used. The watchdog timer, if enabled in the FPGA design, will reset the board if the FPGA fails to toggle the watchdog signal within the configured period.

### 4.3 FTDI USB interface

The FTDI FT4232H (U201) quad-serial USB bridge provides the primary interface between a host computer and the Avant-X70 FPGA for programming, debugging, and communication. The interface is available via the USB-C connector J2. Table 2 lists the port assignment of the FTDI FT4232H.

*Table 2. FTDI FT4232H port assignment on the GR-AVANTX-MINI board.*

Port	Interface	FPGA Signals	Notes
ADBUD (Port 0)	-	-	Not implemented.
BDBUS (Port 1)	JTAG	TCK, TDI, TDO, TMS	FPGA and SPI Flash programming and GRMON4 debugging [RD4].
CDBUS (Port 2)	UART0	RXD0, TXD0	3.3V LVTTTL, console UART.
DDBUS (Port 3)	UART1	RXD1, TXD1	3.3V LVTTTL, secondary UART.

A 12MHz crystal (Y200) provides the FTDI FT4232H a reference clock. A serial EEPROM (U202) stores the FTDI configuration including USB VID/PID and string descriptors. The LDO regulator U200 generates the 3.3V supply for the FT4232H from the USB-C VBUS\_5V rail.

The P LED (D205) lights up green once the FTDI device is powered, enumerated on the host computer, and not in suspend mode. The S LED (D206) lights up red when there is no activity in the USB interface (suspend mode).

#### 4.4 User-accessible interfaces

The GR-AVANTX-MINI board provides different user-accessible controls and indicators as listed in Table 3, Table 4, and Table 5. Different test points are also available on the board. These are presented only on the schematic of the board [RD1].

Table 3. GR-AVANTX-MINI board LEDs.

Reference	Label	Color	Function
D200	3V3	Green	Lights up when the +3V3FT supply is generated.
D1400	POK	Green	Lights up when the power sequencing is completed and reset signal is de-asserted (active low).
D500	DONE	Green	Lights up when FPGA configuration is completed.
D1401	WD	Green	Lights up when the watchdog signal from the FPGA is de-asserted (active low).
D600	LED0	Green	User-programmable.
D601	LED1	Green	User-programmable.
D602	LED2	Green	User-programmable.
D603	LED3	Green	User-programmable.
D205	P	Green	Lights up once the FTDI device is powered, enumerated on the host computer, and not in suspend mode.
D206	S	Red	Lights up when there is no activity in the USB interface (suspend mode).

Table 4. GR-AVANTX-MINI board push buttons.

Reference	Label	Function
S1	RESET	Board master reset.
S2	PROGN	Clears the FPGA configuration or triggers the FPGA configuration from SPI Flash. The function depends on the setting of the MODE jumper (JP2).

Table 5. GR-AVANTX-MINI board jumpers and DIP switches.

Reference	Description	Default	Options
JP1	Board power source	2-3	1-2: dedicated power supply (J1). 2-3: supply from the FTDI cable (J2).
JP2	FPGA configuration mode	Open	Open: controller SPI mode. Closed: JTAG or target SPI mode.
JP3	Watchdog disconnect	Open	Open: watchdog disconnected. Closed: watchdog active.
JP4	VADJ select	Open	Open: 1.2V. 1-2: 1.5V. 2-3: 1.8V.
S3	DIP switches	All off	User-defined pins.

## 5 AVANT-X FPGA

The GR-AVANTX-MINI board uses a Lattice Avant-X70 FPGA (LAV-AT-X70-3LFG676C, U500) in a 676-ball FCBGA package (LFG676, 27x27mm, 1.0mm pitch). The Avant-AT-X is the highest-capability family of the Lattice Avant platform, built on a 16nm FinFET process. Lattice Radiant is the supported design tool for synthesis, place-and-route, timing analysis, Lattice IP generation, and FPGA programming [RD7]. **The Avant-AT-X family is supported in GRLIB from version 2026.2 onward [RD3].**

Table 6 presents the main key features of the Avant-X part used on the GR-AVANTX-MINI board. Additional information about the device can be found in [RD4]. **Appendix B contains the FPGA pin assignment applicable to the board.**

*Table 6. Key features of the Lattice Avant-X70 FPGA used on the GR-AVANTX-MINI board.*

Parameter	Value
Family	Lattice Avant-AT-X
Device	LAV-AT-X70
Part number	LAV-AT-X70-3LFG676C
Package	LFG676 FCBGA, 27x27mm, 1.0mm pitch
Process	16nm FinFET
System Logic Cells (k)	637
LUTs (k)	397
Embedded Memory Blocks (EBR, 36 kb)	990
Embedded Memory (Mb)	35.6
Distributed RAM Bits (kb)	4140
DSP (18x18 Multipliers)	1800
On-chip High Frequency Oscillator	1
General Purpose PLLs (GPLL)	11
Total I/O (WR + HP)	298 (43 wide-range + 255 high-performance)
SerDes lanes (LFG676)	16 (4 quads x 4 lanes)
Core voltage	0.82 V
SerDes max speed	25Gbps per lane
PCIe hard IP	PCIe Gen 4 x8
External memory interfaces	DDR4, LPDDR4, DDR5
Security	AES256-GCM, ECC521, RSA4096, PUF/Unique ID, TRNG, anti-tamper
Configuration modes	Controller SPI (xSPI), Target SPI, JTAG
Soft Error Detection/Correction	Yes (SED/SEC on EBRs and distributed RAM)
Design tool	Lattice Radiant 3.2 or later

### 5.1 Oscillators and clock inputs

Table 7 lists the clock sources provided to the FPGA. Additional clock can be generated in the FPGA design by using the Lattice Avant PLL IP [RD6].

*Table 7. GR-AVANTX-MINI board clock sources.*

Reference	Frequency	Type	FPGA net	Notes
X300	50MHz	LVTTL	CLK50	General clock source.
X301	100MHz	LVTTL	CLK100	General clock source.
X302	100MHz	LVDS	DDRCLK	DDR4 reference clock.
X303	156.25MHz	LVDS	REFCLK	SerDes reference clock.

The CLK50 and CLK100 clocks are routed to a +3V3 FPGA I/O bank. The DDRCLK is routed to the DDR4 memory bank. The REFCLK is routed to the SerDes quads (MPQ0 and MPQ1), which are routed to the FMC+ SerDes interfaces. The DDRCLK P/N polarity is deliberately swapped on the PCB for routing purposes. This must be accounted for in the FPGA design by swapping the differential pair in the pin assignment.

## 5.2 Configuration and programming

The FPGA can be configured either via JTAG (USB-C connector J2, additional information in Sections 4.3 and 5.3) or on-board SPI Flash (U501, additional information in Section 5.4).

The configuration mode depends on the setting of jumper JP2. If JP2 is open (default), the FPGA configuration will be loaded automatically from the external SPI Flash memory (U501) at power-on or after the assertion of the PROGN push button (S2). If JP2 is closed, then the JTAG or target SPI mode configuration is enabled. In this case, asserting the PROGN push button (S2) will clear the FPGA configuration instead of reloading it.

The DONE LED (D500) lights up when the FPGA configuration is completed successfully.

## 5.3 JTAG

JTAG access to the FPGA is provided via the FTDI FT4232H (see Section 4.3). The JTAG signals (TCK, TMS, TDI, TDO) are level-shifted to 3.3V at the FPGA boundary.

Jumper JP2 selects the JTAG configuration mode. In this mode, Lattice Radiant Programmer software [RD7] can be used to program both the FPGA directly and the external SPI Flash memory (U501).

In a GRLIB-based system [RD3], the JTAG interface can also be used to access the design via GRMON4 Debug Monitor [RD5].

No JTAG functionality is implemented on the FMC+ HPC connector.

## 5.4 SPI Flash memory(ies)

Table 8 lists the two SPI Flash memories (Macronix MX25L51245G, WSON5X6 footprint, 3.3V) available on the board and connected to the FPGA.

*Table 8. GR-AVANTX-MINI board SPI Flash memories.*

Reference	FPGA net(s)	Capacity	Function
U501	MS*	512Mb	FPGA configuration.
U1102	SPIM*	512Mb	User data storage.

U501 is connected to the FPGA SPI master interface used by the Lattice sysCONFIG IP [RD8] for FPGA configuration. The memory can be programmed via Lattice Radiant Programmer software

when the FPGA is set in JTAG configuration mode (see Section 5.3). U1102 is connected to the SPI slave user interface for application use is only accessible from an FPGA design.

In order to program the U501 SPI Flash from Lattice Radiant Programmer, the following three steps are required in the correct order<sup>1</sup>:

1. Set the MASTER\_SPI\_PORT value to SERIAL or DUAL in the Radiant Device Constraint Editor (Tools > Device Constraint Editor > Global > sysCONFIG). This prevents the FPGA from holding the dual-function pin RESET#/SIO3 of the memory low when the device is operating in JTAG2SPI bridge mode. It is also recommended to set both MSPI\_ADDRESS\_32BIT and MSPI\_COMMAND\_32BIT to ENABLE.
2. Program the FPGA configuration SRAM (CRAM as target memory) first via JTAG using the Direct Programming access mode in the Lattice Radiant Programmer. The target SPI Flash port will not be accessible before that.
3. Once CRAM programming completes, the user will be able to enumerate and use the U501 SPI Flash in the Lattice Radiant Programmer by changing the target memory to SPI FLASH and the port interface to JTAG2SPI.

## 5.5 DDR4 memory

The FPGA is connected to two DDR4 SDRAM devices (Micron MT40A2G8AG, U1100 and U1101), providing 4GB total of DDR4 memory on a 16-bit data bus.

Intra-byte DQ pin swaps are used on the PCB for routing convenience, in accordance with [RD9]. These swaps are transparent to DDR4 operation because the FPGA DDR4 PHY training operates per-bit within each byte lane.

Table 9, Table 10, and Table 11 list the recommended settings for the Lattice Radiant DDR4 Memory Controller IP [RD11] when using the GR-AVANTX-MINI board. One should note that, according to [RD10], the DDRPHY IP in DDR4 mode has not been fully validated in the Avant-AT-X platform yet. The parameters in the Radiant DDR4 IP configuration interface should be adjusted if link-up or training failures are observed.

*Table 9. GR-AVANTX-MINI board DDR4 parameters – General settings.*

Parameter	Value
Interface type	DDR4
DDR command frequency (MHz)	666
Read latency	10
Write latency	9
Reference clock frequency (MHz)	100
DDR density (per channel)	16Gb
DDR bus width	16
Configuration	x8
Number of ranks	1
Number of DDR clocks	1
Data width	128

<sup>1</sup> Due to the following issue: <https://latticesemiconductor.zohodesk.com/portal/en/kb/articles/avant-rev-03x-how-to-program-quad-spi-flash-programming-issue-using-jtag2spi-bridge>

ID width	4
Maximum burst length	64
Write ordering queues	2
Read ordering queues	2
Enable local bus clock	Yes
Enable APB I/F	Yes

*Table 10. GR-AVANTX-MINI board DDR4 parameters – Memory device timing.*

<b>Parameter</b>	<b>Value</b>
Manual timing adjust enable	Yes
TRCD(tCLK)	10
TRAS(tCLK)	24
TRPPB(tCLK)	10
TWR(tCLK)	17
TRTP(tCLK)	5
TCCD(tCLK)	5
TRRD(tCLK)	4
TRFC(tCLK)	367
TFAW(tCLK)	35
TZQCAL(tCLK)	128
TMRD(tCLK)	8
TRPAB(tCLK)	10
TDQSS(tCLK)	1
TRD2PRE(tCLK)	6
TWR2PRE(tCLK)	30
TXP(tCLK)	4
TXPSR(tCLK)	446
Refresh period (tSCLK)	1298
No. of outstanding refresh	7
ZQ calibration period (sec)	32
ZQ calibration start to latch (usec)	1
Temperature check period (sec)	32

*Table 11. GR-AVANTX-MINI board DDR4 parameters – Training settings.*

<b>Parameter</b>	<b>Value</b>
DDR clock delay value	15
DDR clock delay incr/decr	Yes
CS delay value	15
CS delay value incr/decr	Yes
Address control delay value	4
Address control delay value incr/decr	No
Memory DQ Vref value for rank0	90
MC DQS Grp0 Vref value	80
MC DQS Grp1 Vref value	80
CK/CS slew rate	FAST

Command address slew rate	FAST
DQS slew rate	FAST
DQ/DMI slew rate	FAST
MC CA output impedance	34 Ohm
MC DQ output impedance	34 Ohm
MC ODT value	60 Ohm
RTT_WR value	Dynamic ODT Off
RTT_NOM value	RZQ/5
RTT_PARK value	Disable

On the FPGA design side, the DDRPHY [RD10] should always be trained before it is used. That is accomplished by executing the following four steps:

1. In the reset register of the DDRPHY (RESET\_REG, offset 0x200), write 0x0 ([0] = cpu\_reset\_n).
2. In the training operation register of the DDRPHY (TRN\_OP\_REG, offset 0x220), write 0xDF ([7] = mem\_vref\_training\_en, [6] = mc\_vref\_training\_en, [5] = ca\_vref\_training\_en, [4] = write\_trn\_en, [3] = read\_trn\_en, [2] = write\_lv1\_en, [1] = cbt\_en, [0] = init\_en).
3. In the reset register of the DDRPHY (RESET\_REG, offset 0x200), write 0x1 ([0] = cpu\_reset\_n).
4. Poll the training status register of the DDRPHY (STATUS\_REG, offset 0x224), to confirm that the training was successful. It should return 0x7D ([7] = rank1\_done, [6] = rank0\_done, [5] = scl\_done, [4] = write\_training\_done, [3] = read\_training\_done, [2] = write\_lv1\_done, [1] = cbt\_done, [0] = init\_done).

## 5.6 Ethernet

The FPGA is connected to Gigabit Ethernet PHY (Microchip KSZ9031RNX, U1200) via an RGMII interface. The MDIO address of the PHY is set to 0x3 by pull-up resistors on the board. The PHY is connected to an RJ45 connector (J3) with integrated magnetics and status LEDs.

The operation of the Ethernet PHY at 1Gbps requires configuring the pad skew of the RGMII GTX\_CLK and RX\_CLK clocks via the MDIO interface. That is accomplished by writing 0x001F ([9:5] = GTX\_CLK input pad skew control (0.06ns/step), [4:0] = RX\_CLK output pad skew control (0.06ns/step)) to the RGMII Clock Pad Skew register (MMD Address 2h, Register 8h) of the PHY. Such a configuration is not needed when operating the PHY at 10 and 100Mbps.

## 5.7 SpaceWire

The FPGA is connected to a SpaceWire-capable header on the board (J4, not mounted). The SpaceWire data and strobe LVDS pairs are connected from the FPGA to the header via LVDS buffers/repeaters (U400-3).

To avoid damage to the SpaceWire interface due to common mode voltage, one shall ensure ground equalization between SpaceWire nodes before connecting the board to an equipment.

## 5.8 SerDes

Two SerDes quads (MPQ0 and 1) of the FPGA are routed to the FMC+ HPC connector, providing up to eight SerDes lanes on the board.

By default, the reference clock for both quads is provided by the FMC M2C clock pins. However, it is possible to use the on-board 156.25MHz LVDS oscillator (REFCLK, X303) for that by modifying the configuration of capacitors C825 and C826 on the board.

## 5.9 FMC+ HPC connector

The FPGA is connected to an FMC+ HPC connector (FMC1). The connector provides access to FPGA I/O banks and SerDes interfaces for mezzanine card expansion.

Table 12 provides a summary of the FMC+ HPC connector. Table 13 lists all signals implemented in the connector.

When installing a mezzanine card, verify that its VADJ requirement matches the JP4 setting before powering the board. The GA pins on the connector are set to address 0x0 (no connection to 12V, no connection to VIO\_B\_M2C).

Table 12. FMC+ HPC connector summary.

Resource	Count/Value	Notes
Connector type	FMC+ HPC	ASP-184329-01 (560-pin)
LA differential pairs	34 pairs (LA[33:0])	VADJ bank(s)
HA differential pairs	24 pairs (HA[23:0])	VADJ bank(s)
HB differential pairs	5 pairs (HB[17, 15, 6, 4, 0])	VADJ bank(s)
SerDes lanes	8 (MPQ0 x4 + MPQ1 x4)	TX and RX per lane
SerDes reference clock	156.25MHz LVDS	From FMC M2C CLK or X303
VADJ	1.2/1.5/1.8V	Selectable via JP4 (default 1.2V)
3V3PAUX/3V3P	3.3V	From on-board 3V3 supply
CK_M2C clocks	CK_M2C_P/N[1:0], CK_BD_P/N[1:0]	From FMC card to FPGA
PG_C2M	Power Good	From FPGA/board to FMC card
VREF_A_M2C	VREF signal	From FMC card to FPGA
12P0V	-	Not implemented
I2C	SCL, SDA	3.3V I2C bus shared with FPGA
JTAG	-	Not implemented

Table 13. FMC+ HPC connector pin assignment.

FMC Pin	FMC Signal	Net Name	FPGA Ball	FPGA Bank
A01	GND	DGND		
A02	DP1_M2C_P	DP_M2C_P1	C24	MPQ0
A03	DP1_M2C_N	DP_M2C_N1	C25	MPQ0
A04	GND	DGND		
A05	GND	DGND		
A06	DP2_M2C_P	DP_M2C_P2	A21	MPQ0
A07	DP2_M2C_N	DP_M2C_N2	A22	MPQ0
A08	GND	DGND		
A09	GND	DGND		
A10	DP3_M2C_P	DP_M2C_P3	C21	MPQ0
A11	DP3_M2C_N	DP_M2C_N3	C22	MPQ0

FMC Pin	FMC Signal	Net Name	FPGA Ball	FPGA Bank
A12	GND	DGND		
A13	GND	DGND		
A14	DP4_M2C_P	DP_M2C_P4	A18	MPQ1
A15	DP4_M2C_N	DP_M2C_N4	A19	MPQ1
A16	GND	DGND		
A17	GND	DGND		
A18	DP5_M2C_P	DP_M2C_P5	C18	MPQ1
A19	DP5_M2C_N	DP_M2C_N5	C19	MPQ1
A20	GND	DGND		
A21	GND	DGND		
A22	DP1_C2M_P	DP_C2M_P1	G24	MPQ0
A23	DP1_C2M_N	DP_C2M_N1	G25	MPQ0
A24	GND	DGND		
A25	GND	DGND		
A26	DP2_C2M_P	DP_C2M_P2	E21	MPQ0
A27	DP2_C2M_N	DP_C2M_N2	E22	MPQ0
A28	GND	DGND		
A29	GND	DGND		
A30	DP3_C2M_P	DP_C2M_P3	G21	MPQ0
A31	DP3_C2M_N	DP_C2M_N3	G22	MPQ0
A32	GND	DGND		
A33	GND	DGND		
A34	DP4_C2M_P	DP_C2M_P4	E18	MPQ1
A35	DP4_C2M_N	DP_C2M_N4	E19	MPQ1
A36	GND	DGND		
A37	GND	DGND		
A38	DP5_C2M_P	DP_C2M_P5	G18	MPQ1
A39	DP5_C2M_N	DP_C2M_N5	G19	MPQ1
A40	GND	DGND		
B01	FMC_CLK_DIR	FMC_CLK_DIR		
B02	GND	DGND		
B03	GND	DGND		
B04	DP9_M2C_P			
B05	DP9_M2C_N			
B06	GND	DGND		
B07	GND	DGND		
B08	DP8_M2C_P			
B09	DP8_M2C_N			
B10	GND	DGND		
B11	GND	DGND		
B12	DP7_M2C_P	DP_M2C_P7	C15	MPQ1
B13	DP7_M2C_N	DP_M2C_N7	C16	MPQ1

FMC Pin	FMC Signal	Net Name	FPGA Ball	FPGA Bank
B14	GND	DGND		
B15	GND	DGND		
B16	DP6_M2C_P	DP_M2C_P6	A15	MPQ1
B17	DP6_M2C_N	DP_M2C_N6	A16	MPQ1
B18	GND	DGND		
B19	GND	DGND		
B20	GBTCLK1_M2C_P	GC_M2C_P1	J18	MPQ1
B21	GBTCLK1_M2C_N	GC_M2C_N1	J19	MPQ1
B22	GND	DGND		
B23	GND	DGND		
B24	DP9_C2M_P			
B25	DP9_C2M_N			
B26	GND	DGND		
B27	GND	DGND		
B28	DP8_C2M_P			
B29	DP8_C2M_N			
B30	GND	DGND		
B31	GND	DGND		
B32	DP7_C2M_P	DP_C2M_P7	G15	MPQ1
B33	DP7_C2M_N	DP_C2M_N7	G16	MPQ1
B34	GND	DGND		
B35	GND	DGND		
B36	DP6_C2M_P	DP_C2M_P6	E15	MPQ1
B37	DP6_C2M_N	DP_C2M_N6	E16	MPQ1
B38	GND	DGND		
B39	GND	DGND		
B40	RES0	RES0 (not connected)		
C01	GND	GND		
C02	DP0_C2M_P	DP_C2M_P0	E24	MPQ0
C03	DP0_C2M_N	DP_C2M_N0	E25	MPQ0
C04	GND	DGND		
C05	GND	DGND		
C06	DP0_M2C_P	DP_M2C_P0	A24	MPQ0
C07	DP0_M2C_N	DP_M2C_N0	A25	MPQ0
C08	GND	DGND		
C09	GND	DGND		
C10	LA06_P	LA_P6	W14	BANK8
C11	LA06_N	LA_N6	Y14	BANK8
C12	GND	DGND		
C13	GND	DGND		
C14	LA10_P	LA_P10	W10	BANK3
C15	LA10_N	LA_N10	V11	BANK3

FMC Pin	FMC Signal	Net Name	FPGA Ball	FPGA Bank
C16	GND	DGND		
C17	GND	DGND		
C18	LA14_P	LA_P14	Y8	BANK8
C19	LA14_N	LA_N14	Y9	BANK8
C20	GND	DGND		
C21	GND	DGND		
C22	LA18_P_CC	LA_P18	AB3	BANK3
C23	LA18_N_CC	LA_N18	AB4	BANK3
C24	GND	DGND		
C25	GND	DGND		
C26	LA27_P	LA_P27	AE4	BANK3
C27	LA27_N	LA_N27	AE5	BANK3
C28	GND	DGND		
C29	GND	DGND		
C30	SCL	FMC_SCL	R2	BANK2
C31	SDA	FMC_SDA	R1	BANK2
C32	GND	DGND		
C33	GND	DGND		
C34	GA0	DGND		
C35	12P0V			
C36	GND	DGND		
C37	12P0V			
C38	GND	DGND		
C39	3P3V	3V3P		
C40	GND	DGND		
D01	PG_C2M	PG_C2M		
D02	GND	DGND		
D03	GND	DGND		
D04	GBTCLK0_M2C_P	GC_M2C_P0	J24	MPQ0
D05	GBTCLK0_M2C_N	GC_M2C_N0	J25	MPQ0
D06	GND	DGND		
D07	GND	DGND		
D08	LA01_P_CC	LA_P1	AA6	BANK3
D09	LA01_N_CC	LA_N1	AA7	BANK3
D10	GND	DGND		
D11	LA05_P	LA_P5	W13	BANK8
D12	LA05_N	LA_N5	Y13	BANK8
D13	GND	DGND		
D14	LA09_P	LA_P9	Y12	BANK8
D15	LA09_N	LA_N9	W12	BANK8
D16	GND	DGND		
D17	LA13_P	LA_P13	V10	BANK3

FMC Pin	FMC Signal	Net Name	FPGA Ball	FPGA Bank
D18	LA13_N	LA_N13	V9	BANK3
D19	GND	DGND		
D20	LA17_P_CC	LA_P17	W4	BANK3
D21	LA17_N_CC	LA_N17	V4	BANK3
D22	GND	DGND		
D23	LA23_P	LA_P23	AB8	BANK8
D24	LA23_N	LA_N23	AA8	BANK8
D25	GND	DGND		
D26	LA26_P	LA_P26	Y6	BANK3
D27	LA26_N	LA_N26	Y7	BANK3
D28	GND	DGND		
D29	TCK	TCK1 (not connected)		
D30	TDI	TDI1 (not connected)		
D31	TDO	TDO1 (not connected)		
D32	3P3VAUX	3V3PAUX		
D33	TMS	TMS1 (not connected)		
D34	TRST_L	TRSTN1 (not connected)		
D35	GA1	DGND		
D36	3P3V	3V3P		
D37	GND	DGND		
D38	3P3V	3V3P		
D39	GND	DGND		
D40	3P3V	3V3P		
E01	GND	DGND		
E02	HA01_P_CC	HA_P1	AE14	BANK9
E03	HA01_N_CC	HA_N1	AF14	BANK9
E04	GND	DGND		
E05	GND	DGND		
E06	HA05_P	HA_P5	AE18	BANK9
E07	HA05_N	HA_N5	AF18	BANK9
E08	GND	DGND		
E09	HA09_P	HA_P9	AB17	BANK9
E10	HA09_N	HA_N9	AC17	BANK9
E11	GND	DGND		
E12	HA13_P	HA_P13	P18	BANK9
E13	HA13_N	HA_N13	N18	BANK9
E14	GND	DGND		
E15	HA16_P	HA_P16	AA15	BANK9
E16	HA16_N	HA_N16	AB15	BANK9
E17	GND	DGND		
E18	HA20_P	HA_P20	U15	BANK9
E19	HA20_N	HA_N20	T15	BANK9

FMC Pin	FMC Signal	Net Name	FPGA Ball	FPGA Bank
E20	GND	DGND		
E21	HB03_P			
E22	HB03_N			
E23	GND	DGND		
E24	HB05_P			
E25	HB05_N			
E26	GND	DGND		
E27	HB09_P			
E28	HB09_N			
E29	GND	DGND		
E30	HB13_P			
E31	HB13_N			
E32	GND	DGND		
E33	HB19_P			
E34	HB19_N			
E35	GND	DGND		
E36	HB21_P			
E37	HB21_N			
E38	GND	DGND		
E39	VADJ	VADJ		
E40	GND	DGND		
F01	PG_M2C	PG_M2C	P6	BANK1
F02	GND	DGND		
F03	GND	DGND		
F04	HA00_P_CC	HA_P0	AE19	BANK9
F05	HA00_N_CC	HA_N0	AF19	BANK9
F06	GND	DGND		
F07	HA04_P	HA_P4	AE17	BANK9
F08	HA04_N	HA_N4	AF17	BANK9
F09	GND	DGND		
F10	HA08_P	HA_P8	AA18	BANK9
F11	HA08_N	HA_N8	AB18	BANK9
F12	GND	DGND		
F13	HA12_P	HA_P12	Y17	BANK9
F14	HA12_N	HA_N12	Y16	BANK9
F15	GND	DGND		
F16	HA15_P	HA_P15	P15	BANK9
F17	HA15_N	HA_N15	R15	BANK9
F18	GND	DGND		
F19	HA19_P	HA_P19	P16	BANK9
F20	HA19_N	HA_N19	R16	BANK9
F21	GND	DGND		

FMC Pin	FMC Signal	Net Name	FPGA Ball	FPGA Bank
F22	HB02_P			
F23	HB02_N			
F24	GND	DGND		
F25	HB04_P	HB04_P	V6	BANK3
F26	HB04_N	HB04_N	V5	BANK3
F27	GND	DGND		
F28	HB08_P			
F29	HB08_N			
F30	GND	DGND		
F31	HB12_P			
F32	HB12_N			
F33	GND	DGND		
F34	HB16_P			
F35	HB16_N			
F36	GND	DGND		
F37	HB20_P			
F38	HB20_N			
F39	GND	DGND		
F40	VADJ	VADJ		
G01	GND	DGND		
G02	CLK1_M2C_P	CK_M2C_P1	AC9	BANK8
G03	CLK1_M2C_N	CK_M2C_N1	AD9	BANK8
G04	GND	DGND		
G05	GND	DGND		
G06	LA00_P_CC	LA_P0	AA2	BANK3
G07	LA00_N_CC	LA_N0	AA1	BANK3
G08	GND	DGND		
G09	LA03_P	LA_P3	AE13	BANK8
G10	LA03_N	LA_N3	AF13	BANK8
G11	GND	DGND		
G12	LA08_P	LA_P8	AC11	BANK8
G13	LA08_N	LA_N8	AC12	BANK8
G14	GND	DGND		
G15	LA12_P	LA_P12	AF6	BANK8
G16	LA12_N	LA_N12	AF7	BANK8
G17	GND	DGND		
G18	LA16_P	LA_P16	AC14	BANK8
G19	LA16_N	LA_N16	AD14	BANK8
G20	GND	DGND		
G21	LA20_P	LA_P20	AD8	BANK8
G22	LA20_N	LA_N20	AC8	BANK8
G23	GND	DGND		

FMC Pin	FMC Signal	Net Name	FPGA Ball	FPGA Bank
G24	LA22_P	LA_P22	AD7	BANK8
G25	LA22_N	LA_N22	AD6	BANK8
G26	GND	DGND		
G27	LA25_P	LA_P25	AC4	BANK3
G28	LA25_N	LA_N25	AC3	BANK3
G29	GND	DGND		
G30	LA29_P	LA_P29	W2	BANK3
G31	LA29_N	LA_N29	W1	BANK3
G32	GND	DGND		
G33	LA31_P	LA_P31	AB1	BANK3
G34	LA31_N	LA_N31	AB2	BANK3
G35	GND	DGND		
G36	LA33_P	LA_P33	AD1	BANK3
G37	LA33_N	LA_N33	AD2	BANK3
G38	GND	DGND		
G39	VADJ	VADJ		
G40	GND	DGND		
H01	VREF_A_M2C	VREF_A_M2C	Y4/Y10/P17	BANK3/8/9
H02	PRSNT_M2C_L	FMC_PRSNTN	R3	BANK1
H03	GND	DGND		
H04	CLK0_M2C_P	CK_M2C_P0	AC7	BANK8
H05	CLK0_M2C_N	CK_M2C_N0	AB7	BANK8
H06	GND	DGND		
H07	LA02_P	LA_P2	AB13	BANK8
H08	LA02_N	LA_N2	AB12	BANK8
H09	GND	DGND		
H10	LA04_P	LA_P4	AE12	BANK8
H11	LA04_N	LA_N4	AF12	BANK8
H12	GND	DGND		
H13	LA07_P	LA_P7	AF9	BANK8
H14	LA07_N	LA_N7	AF8	BANK8
H15	GND	DGND		
H16	LA11_P	LA_P11	AF5	BANK3
H17	LA11_N	LA_N11	AF4	BANK3
H18	GND	DGND		
H19	LA15_P	LA_P15	AF2	BANK3
H20	LA15_N	LA_N15	AF3	BANK3
H21	GND	DGND		
H22	LA19_P	LA_P19	W8	BANK3
H23	LA19_N	LA_N19	W9	BANK3
H24	GND	DGND		
H25	LA21_P	LA_P21	AE6	BANK8

FMC Pin	FMC Signal	Net Name	FPGA Ball	FPGA Bank
H26	LA21_N	LA_N21	AE7	BANK8
H27	GND	DGND		
H28	LA24_P	LA_P24	V2	BANK3
H29	LA24_N	LA_N24	V1	BANK3
H30	GND	DGND		
H31	LA28_P	LA_P28	Y2	BANK3
H32	LA28_N	LA_N28	Y1	BANK3
H33	GND	DGND		
H34	LA30_P	LA_P30	AC1	BANK3
H35	LA30_N	LA_N30	AC2	BANK3
H36	GND	DGND		
H37	LA32_P	LA_P32	AE2	BANK3
H38	LA32_N	LA_N32	AE1	BANK3
H39	GND	DGND		
H40	VADJ	VADJ		
J01	GND	DGND		
J02	CLK3_BIDIR_P	CK_BD_P3	AE10	BANK8
J03	CLK3_BIDIR_N	CK_BD_N3	AF10	BANK8
J04	GND	DGND		
J05	GND	DGND		
J06	HA03_P	HA_P3	L18	BANK9
J07	HA03_N	HA_N3	M18	BANK9
J08	GND	DGND		
J09	HA07_P	HA_P7	W16	BANK9
J10	HA07_N	HA_N7	V15	BANK9
J11	GND	DGND		
J12	HA11_P	HA_P11	L16	BANK9
J13	HA11_N	HA_N11	M16	BANK9
J14	GND	DGND		
J15	HA14_P	HA_P14	T16	BANK9
J16	HA14_N	HA_N14	T17	BANK9
J17	GND	DGND		
J18	HA18_P	HA_P18	AE15	BANK9
J19	HA18_N	HA_N18	AF15	BANK9
J20	GND	DGND		
J21	HA22_P	HA_P22	N15	BANK9
J22	HA22_N	HA_N22	M15	BANK9
J23	GND	DGND		
J24	HB01_P			
J25	HB01_N			
J26	GND	DGND		
J27	HB07_P			

FMC Pin	FMC Signal	Net Name	FPGA Ball	FPGA Bank
J28	HB07_N			
J29	GND	DGND		
J30	HB11_P			
J31	HB11_N			
J32	GND	DGND		
J33	HB15_P	HB15_P	AC5	BANK3
J34	HB15_N	HB15_N	AC6	BANK3
J35	GND	DGND		
J36	HB18_P			
J37	HB18_N			
J38	GND	DGND		
J39	VIO_B_M2C			
J40	GND	DGND		
K01	VREF_B_M2C	VREF_B_M2C (not connected)		
K02	GND	DGND		
K03	GND	DGND		
K04	CLK2_BIDIR_P	CK_BD_P2	Y15	BANK8
K05	CLK2_BIDIR_N	CK_BD_N2	W15	BANK8
K06	GND	DGND		
K07	HA02_P	HA_P2	L17	BANK9
K08	HA02_N	HA_N2	M17	BANK9
K09	GND	DGND		
K10	HA06_P	HA_P6	AC18	BANK9
K11	HA06_N	HA_N6	AD18	BANK9
K12	GND	DGND		
K13	HA10_P	HA_P10	AD15	BANK9
K14	HA10_N	HA_N10	AC15	BANK9
K15	GND	DGND		
K16	HA17_P_CC	HA_P17	AB16	BANK9
K17	HA17_N_CC	HA_N17	AC16	BANK9
K18	GND	DGND		
K19	HA21_P	HA_P21	T18	BANK9
K20	HA21_N	HA_N21	R18	BANK9
K21	GND	DGND		
K22	HA23_P	HA_P23	AE16	BANK9
K23	HA23_N	HA_N23	AF16	BANK9
K24	GND	DGND		
K25	HB00_P_CC	HB00_P	W5	BANK3
K26	HB00_N_CC	HB00_N	W6	BANK3
K27	GND	DGND		
K28	HB06_P_CC	HB06_P	AB5	BANK3

FMC Pin	FMC Signal	Net Name	FPGA Ball	FPGA Bank
K29	HB06_N_CC	HB06_N	AB6	BANK3
K30	GND	DGND		
K31	HB10_P			
K32	HB10_N			
K33	GND	DGND		
K34	HB14_P			
K35	HB14_N			
K36	GND	DGND		
K37	HB17_P_CC	HB17_P	AD5	BANK3
K38	HB17_N_CC	HB17_N	AD4	BANK3
K39	GND	DGND		
K40	VIO_B_M2C			
L01	RES1	RES1 (not connected)		
L02	GND	DGND		
L03	GND	DGND		
L04	GBTCL0K4_M2C_P			
L05	GBTCL0K4_M2C_N			
L06	GND	DGND		
L07	GND	DGND		
L08	GBTCL0K3_M2C_P			
L09	GBTCL0K3_M2C_N			
L10	GND	DGND		
L11	GND	DGND		
L12	GBTCLK2_M2C_P			
L13	GBTCLK2_M2C_N			
L14	GND	DGND		
L15	GND	DGND		
L16	SYNC_C2M_P			
L17	SYNC_C2M_N			
L18	GND	DGND		
L19	GND	DGND		
L20	REFCLK_C2M_P			
L21	REFCLK_C2M_N			
L22	GND	DGND		
L23	GND	DGND		
L24	REFCLK_M2C_P			
L25	REFCLK_M2C_N			
L26	GND	DGND		
L27	GND	DGND		
L28	SYNC_M2C_P			
L29	SYNC_M2C_N			
L30	GND	DGND		

FMC Pin	FMC Signal	Net Name	FPGA Ball	FPGA Bank
L31	GND	DGND		
L32	RES2	RES2		
L33	RES3	RES3		
L34	GND	DGND		
L35	GND	DGND		
L36	12P0V			
L37	12P0V			
L38	GND	DGND		
L39	GND	DGND		
L40	12P0V			
M01	GND	DGND		
M02	DP23_M2C_P			
M03	DP23_M2C_N			
M04	GND	DGND		
M05	GND	DGND		
M06	DP22_M2C_P			
M07	DP22_M2C_N			
M08	GND	DGND		
M09	GND	DGND		
M10	DP21_M2C_P			
M11	DP21_M2C_N			
M12	GND	DGND		
M13	GND	DGND		
M14	DP20_M2C_P			
M15	DP20_M2C_N			
M16	GND	DGND		
M17	GND	DGND		
M18	DP14_C2M_P			
M19	DP14_C2M_N			
M20	GND	DGND		
M21	GND	DGND		
M22	DP15_C2M_P			
M23	DP15_C2M_N			
M24	GND	DGND		
M25	GND	DGND		
M26	DP16_C2M_P			
M27	DP16_C2M_N			
M28	GND	DGND		
M29	GND	DGND		
M30	DP17_C2M_P			
M31	DP17_C2M_N			
M32	GND	DGND		

FMC Pin	FMC Signal	Net Name	FPGA Ball	FPGA Bank
M33	GND	DGND		
M34	DP18_C2M_P			
M35	DP18_C2M_N			
M36	GND	DGND		
M37	GND	DGND		
M38	DP19_C2M_P			
M39	DP19_C2M_N			
M40	GND	DGND		
Y01	GND	DGND		
Y02	DP23_C2M_P			
Y03	DP23_C2M_N			
Y04	GND	DGND		
Y05	GND	DGND		
Y06	DP21_C2M_P			
Y07	DP21_C2M_N			
Y08	GND	DGND		
Y09	GND	DGND		
Y10	DP10_M2C_P			
Y11	DP10_M2C_N			
Y12	GND	DGND		
Y13	GND	DGND		
Y14	DP12_M2C_P			
Y15	DP12_M2C_N			
Y16	GND	DGND		
Y17	GND	DGND		
Y18	DP14_M2C_P			
Y19	DP14_M2C_N			
Y20	GND	DGND		
Y21	GND	DGND		
Y22	DP15_M2C_P			
Y23	DP15_M2C_N			
Y24	GND	DGND		
Y25	GND	DGND		
Y26	DP11_C2M_P			
Y27	DP11_C2M_N			
Y28	GND	DGND		
Y29	GND	DGND		
Y30	DP13_C2M_P			
Y31	DP13_C2M_N			
Y32	GND	DGND		
Y33	GND	DGND		
Y34	DP17_M2C_P			

FMC Pin	FMC Signal	Net Name	FPGA Ball	FPGA Bank
Y35	DP17_M2C_N			
Y36	GND	DGND		
Y37	GND	DGND		
Y38	DP19_M2C_P			
Y39	DP19_M2C_N			
Y40	GND	DGND		
Z01	PRSNT_M2C_L			
Z02	GND	DGND		
Z03	GND	DGND		
Z04	DP22_C2M_P			
Z05	DP22_C2M_N			
Z06	GND	DGND		
Z07	GND	DGND		
Z08	DP20_C2M_P			
Z09	DP20_C2M_N			
Z10	GND	DGND		
Z11	GND	DGND		
Z12	DP11_M2C_P			
Z13	DP11_M2C_N			
Z14	GND	DGND		
Z15	GND	DGND		
Z16	DP13_M2C_P			
Z17	DP13_M2C_N			
Z18	GND	DGND		
Z19	GND	DGND		
Z20	GBTCLK5_M2C_P			
Z21	GBTCLK5_M2C_N			
Z22	GND	DGND		
Z23	GND	DGND		
Z24	DP10_C2M_P			
Z25	DP10_C2M_N			
Z26	GND	DGND		
Z27	GND	DGND		
Z28	DP12_C2M_P			
Z29	DP12_C2M_N			
Z30	GND	DGND		
Z31	GND	DGND		
Z32	DP16_M2C_P			
Z33	DP16_M2C_N			
Z34	GND	DGND		
Z35	GND	DGND		
Z36	DP18_M2C_P			

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<b>FMC Pin</b>	<b>FMC Signal</b>	<b>Net Name</b>	<b>FPGA Ball</b>	<b>FPGA Bank</b>
Z37	DP18_M2C_N			
Z38	GND	DGND		
Z39	GND	DGND		
Z40	3P3V	3V3P		

**APPENDIX A – BOARD ASSEMBLY DRAWING**

View from Top side (Scale 2:1)

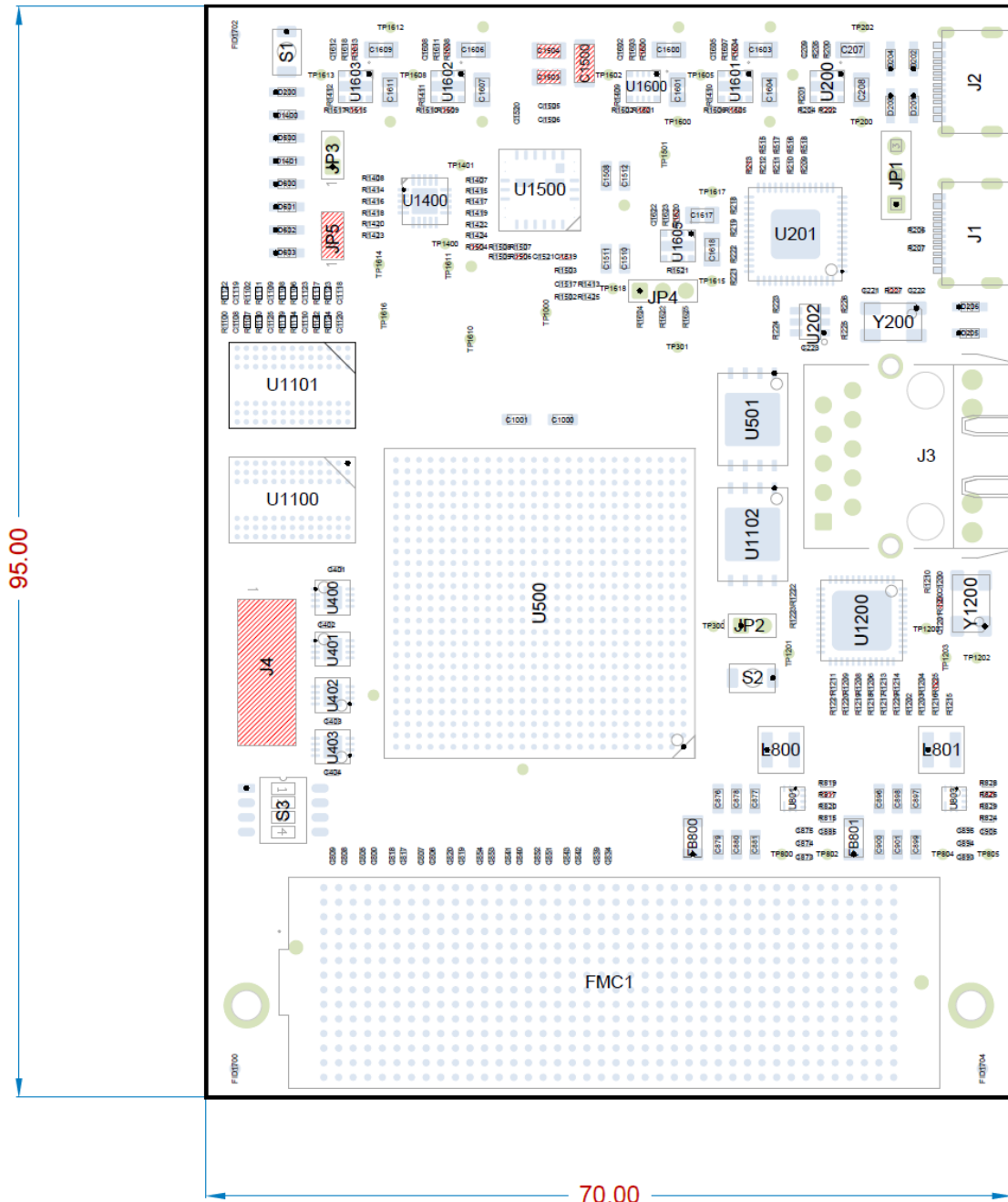


Figure 4. Top view of the GR-AVANTX-MINI board.



Figure 5. Bottom view of the GR-AVANTX-MINI board.

**APPENDIX B – FPGA PIN ASSIGNMENT**

*Table 14. FPGA pin assignment of the Lattice Avant-X70 FPGA (LAV-AT-X70-3LFG676C) on the GR-AVANTX-MINI board.*

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
A1	VSS	DGND	DGND	
A2	MPQ3_RX2P	DGND	DGND	
A3	MPQ3_RX2N	DGND	DGND	
A4	VSS	DGND	DGND	
A5	MPQ3_RX0P	DGND	DGND	
A6	MPQ3_RX0N	DGND	DGND	
A7	VSS	DGND	DGND	
A8	MPQ2_RX2P	DGND	DGND	
A9	MPQ2_RX2N	DGND	DGND	
A10	VSS	DGND	DGND	
A11	MPQ2_RX0P	DGND	DGND	
A12	MPQ2_RX0N	DGND	DGND	
A13	VSS	DGND	DGND	
A14	VSS	DGND	DGND	
A15	MPQ1_RX2P	DP_P6	FMC+ HPC	DP6_M2C_P
A16	MPQ1_RX2N	DP_N6	FMC+ HPC	DP6_M2C_N
A17	VSS	DGND	DGND	
A18	MPQ1_RX0P	DP_P4	FMC+ HPC	DP4_M2C_P
A19	MPQ1_RX0N	DP_N4	FMC+ HPC	DP4_M2C_N
A20	VSS	DGND	DGND	
A21	MPQ0_RX2P	DP_P2	FMC+ HPC	DP2_M2C_P
A22	MPQ0_RX2N	DP_N2	FMC+ HPC	DP2_M2C_N
A23	VSS	DGND	DGND	
A24	MPQ0_RX0P	DP_P0	FMC+ HPC	DP0_M2C_P
A25	MPQ0_RX0N	DP_N0	FMC+ HPC	DP0_M2C_N
A26	VSS	DGND	DGND	
B1	VCCH_MPQ3	DGND	DGND	
B2	VSS	DGND	DGND	
B3	VSS	DGND	DGND	
B4	VCCH_MPQ3	DGND	DGND	
B5	VSS	DGND	DGND	
B6	VSS	DGND	DGND	
B7	VCCH_MPQ2	DGND	DGND	
B8	VSS	DGND	DGND	
B9	VSS	DGND	DGND	
B10	VCCH_MPQ2	DGND	DGND	
B11	VSS	DGND	DGND	
B12	VSS	DGND	DGND	

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
B13	VCCH_MPQ2	DGND	DGND	
B14	VCCH_MPQ1	VCCH_MPQ1	PWR	VCCH_MPQ1
B15	VSS	DGND	DGND	
B16	VSS	DGND	DGND	
B17	VCCH_MPQ1	VCCH_MPQ1	PWR	VCCH_MPQ1
B18	VSS	DGND	DGND	
B19	VSS	DGND	DGND	
B20	VCCH_MPQ0	VCCH_MPQ0	PWR	VCCH_MPQ0
B21	VSS	DGND	DGND	
B22	VSS	DGND	DGND	
B23	VCCH_MPQ0	VCCH_MPQ0	PWR	VCCH_MPQ0
B24	VSS	DGND	DGND	
B25	VSS	DGND	DGND	
B26	VCCH_MPQ0	VCCH_MPQ0	PWR	VCCH_MPQ0
C1	VSS	DGND	DGND	
C2	MPQ3_RX3P	DGND	DGND	
C3	MPQ3_RX3N	DGND	DGND	
C4	VSS	DGND	DGND	
C5	MPQ3_RX1P	DGND	DGND	
C6	MPQ3_RX1N	DGND	DGND	
C7	VSS	DGND	DGND	
C8	MPQ2_RX3P	DGND	DGND	
C9	MPQ2_RX3N	DGND	DGND	
C10	VSS	DGND	DGND	
C11	MPQ2_RX1P	DGND	DGND	
C12	MPQ2_RX1N	DGND	DGND	
C13	VSS	DGND	DGND	
C14	VSS	DGND	DGND	
C15	MPQ1_RX3P	DP_P7	FMC+ HPC	DP7_M2C_P
C16	MPQ1_RX3N	DP_N7	FMC+ HPC	DP7_M2C_N
C17	VSS	DGND	DGND	
C18	MPQ1_RX1P	DP_P5	FMC+ HPC	DP5_M2C_P
C19	MPQ1_RX1N	DP_N5	FMC+ HPC	DP5_M2C_N
C20	VSS	DGND	DGND	
C21	MPQ0_RX3P	DP_P3	FMC+ HPC	DP3_M2C_P
C22	MPQ0_RX3N	DP_N3	FMC+ HPC	DP3_M2C_N
C23	VSS	DGND	DGND	
C24	MPQ0_RX1P	DP_P1	FMC+ HPC	DP1_M2C_P
C25	MPQ0_RX1N	DP_N1	FMC+ HPC	DP1_M2C_N
C26	VSS	DGND	DGND	
D1	VCCH_MPQ3	DGND	DGND	
D2	VSS	DGND	DGND	

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
D3	VSS	DGND	DGND	
D4	VCCH_MPQ3	DGND	DGND	
D5	VSS	DGND	DGND	
D6	VSS	DGND	DGND	
D7	VCCH_MPQ3	DGND	DGND	
D8	VSS	DGND	DGND	
D9	VSS	DGND	DGND	
D10	VCCH_MPQ2	DGND	DGND	
D11	VSS	DGND	DGND	
D12	VSS	DGND	DGND	
D13	VCCH_MPQ2	DGND	DGND	
D14	VCCH_MPQ1	VCCH_MPQ1	PWR	VCCH_MPQ1
D15	VSS	DGND	DGND	
D16	VSS	DGND	DGND	
D17	VCCH_MPQ1	VCCH_MPQ1	PWR	VCCH_MPQ1
D18	VSS	DGND	DGND	
D19	VSS	DGND	DGND	
D20	VCCH_MPQ1	VCCH_MPQ1	PWR	VCCH_MPQ1
D21	VSS	DGND	DGND	
D22	VSS	DGND	DGND	
D23	VCCH_MPQ0	VCCH_MPQ0	PWR	VCCH_MPQ0
D24	VSS	DGND	DGND	
D25	VSS	DGND	DGND	
D26	VCCH_MPQ0	VCCH_MPQ0	PWR	VCCH_MPQ0
E1	VSS	DGND	DGND	
E2	NC	NC	NC	
E3	NC	NC	NC	
E4	VSS	DGND	DGND	
E5	NC	NC	NC	
E6	NC	NC	NC	
E7	VSS	DGND	DGND	
E8	NC	NC	NC	
E9	NC	NC	NC	
E10	VSS	DGND	DGND	
E11	NC	NC	NC	
E12	NC	NC	NC	
E13	VSS	DGND	DGND	
E14	VSS	DGND	DGND	
E15	MPQ1_TX2P	DP_C2M_P6	FMC+ HPC	DP6_C2M_P
E16	MPQ1_TX2N	DP_C2M_N6	FMC+ HPC	DP6_C2M_N
E17	VSS	DGND	DGND	
E18	MPQ1_TX0P	DP_C2M_P4	FMC+ HPC	DP4_C2M_P

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
E19	MPQ1_TX0N	DP_C2M_N4	FMC+ HPC	DP4_C2M_N
E20	VSS	DGND	DGND	
E21	MPQ0_TX2P	DP_C2M_P2	FMC+ HPC	DP2_C2M_P
E22	MPQ0_TX2N	DP_C2M_N2	FMC+ HPC	DP2_C2M_N
E23	VSS	DGND	DGND	
E24	MPQ0_TX0P	DP_C2M_P0	FMC+ HPC	DP0_C2M_P
E25	MPQ0_TX0N	DP_C2M_N0	FMC+ HPC	DP0_C2M_N
E26	VSS	DGND	DGND	
F1	VCCA_MPQ3	DGND	DGND	
F2	VSS	DGND	DGND	
F3	VSS	DGND	DGND	
F4	VCCA_MPQ3	DGND	DGND	
F5	VSS	DGND	DGND	
F6	VSS	DGND	DGND	
F7	VCCA_MPQ2	DGND	DGND	
F8	VSS	DGND	DGND	
F9	VSS	DGND	DGND	
F10	VCCA_MPQ2	DGND	DGND	
F11	VSS	DGND	DGND	
F12	VSS	DGND	DGND	
F13	VCCA_MPQ2	DGND	DGND	
F14	VCCA_MPQ1	VCCA_MPQ1	PWR	VCCA_MPQ1
F15	VSS	DGND	DGND	
F16	VSS	DGND	DGND	
F17	VCCA_MPQ1	VCCA_MPQ1	PWR	VCCA_MPQ1
F18	VSS	DGND	DGND	
F19	VSS	DGND	DGND	
F20	VCCA_MPQ1	VCCA_MPQ1	PWR	VCCA_MPQ1
F21	VSS	DGND	DGND	
F22	VSS	DGND	DGND	
F23	VCCA_MPQ0	VCCA_MPQ0	PWR	VCCA_MPQ0
F24	VSS	DGND	DGND	
F25	VSS	DGND	DGND	
F26	VCCA_MPQ0	VCCA_MPQ0	PWR	VCCA_MPQ0
G1	VSS	DGND	DGND	
G2	NC	NC	NC	
G3	NC	NC	NC	
G4	VSS	DGND	DGND	
G5	NC	NC	NC	
G6	NC	NC	NC	
G7	VSS	DGND	DGND	
G8	NC	NC	NC	

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
G9	NC	NC	NC	
G10	VSS	DGND	DGND	
G11	NC	NC	NC	
G12	NC	NC	NC	
G13	VSS	DGND	DGND	
G14	VSS	DGND	DGND	
G15	MPQ1_TX3P	DP_C2M_P7	FMC+ HPC	DP7_C2M_P
G16	MPQ1_TX3N	DP_C2M_N7	FMC+ HPC	DP7_C2M_N
G17	VSS	DGND	DGND	
G18	MPQ1_TX1P	DP_C2M_P5	FMC+ HPC	DP5_C2M_P
G19	MPQ1_TX1N	DP_C2M_N5	FMC+ HPC	DP5_C2M_N
G20	VSS	DGND	DGND	
G21	MPQ0_TX3P	DP_C2M_P3	FMC+ HPC	DP3_C2M_P
G22	MPQ0_TX3N	DP_C2M_N3	FMC+ HPC	DP3_C2M_N
G23	VSS	DGND	DGND	
G24	MPQ0_TX1P	DP_C2M_P1	FMC+ HPC	DP1_C2M_P
G25	MPQ0_TX1N	DP_C2M_N1	FMC+ HPC	DP1_C2M_N
G26	VSS	DGND	DGND	
H1	VCCA_MPQ3	DGND	DGND	
H2	VSS	DGND	DGND	
H3	VSS	DGND	DGND	
H4	VCCA_MPQ3	DGND	DGND	
H5	VSS	DGND	DGND	
H6	VSS	DGND	DGND	
H7	VCCA_MPQ3	DGND	DGND	
H8	VSS	DGND	DGND	
H9	VSS	DGND	DGND	
H10	VCCA_MPQ3	DGND	DGND	
H11	VSS	DGND	DGND	
H12	VSS	DGND	DGND	
H13	VCCA_MPQ2	DGND	DGND	
H14	VCCA_MPQ2	DGND	DGND	
H15	VSS	DGND	DGND	
H16	VSS	DGND	DGND	
H17	VCCA_MPQ1	VCCA_MPQ1	PWR	VCCA_MPQ1
H18	VSS	DGND	DGND	
H19	VSS	DGND	DGND	
H20	VCCA_MPQ0	VCCA_MPQ0	PWR	VCCA_MPQ0
H21	VSS	DGND	DGND	
H22	VSS	DGND	DGND	
H23	VCCA_MPQ0	VCCA_MPQ0	PWR	VCCA_MPQ0
H24	VSS	DGND	DGND	

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
H25	VSS	DGND	DGND	
H26	VCCA_MPQ0	VCCA_MPQ0	PWR	VCCA_MPQ0
J1	VSS	DGND	DGND	
J2	MPQ3_REFCLKP	DGND	DGND	
J3	MPQ3_REFCLKN	DGND	DGND	
J4	VSS	DGND	DGND	
J5	REXT_MPQ3	DGND	DGND	
J6	VCCIO2	+3V3	PWR	+3V3
J7	VSS	DGND	DGND	
J8	VCCH_MPQ3	DGND	DGND	
J9	REXT_MPQ2	DGND	DGND	
J10	VSS	DGND	DGND	
J11	MPQ2_REFCLKP	DGND	DGND	
J12	MPQ2_REFCLKN	DGND	DGND	
J13	VSS	DGND	DGND	
J14	VCCA_MPQ3	DGND	DGND	
J15	VCCA_MPQ2	DGND	DGND	
J16	REXT_MPQ1	DGND	DGND	
J17	VSS	DGND	DGND	
J18	MPQ1_REFCLKP	MPQ_REF-CLK P1	FMC+ HPC	GBTCLK1_M2C_P
J19	MPQ1_REFCLKN	MPQ_REF-CLK N1	FMC+ HPC	GBTCLK1_M2C_N
J20	VSS	DGND	DGND	
J21	VCCA_MPQ0	VCCA_MPQ0	PWR	VCCA_MPQ0
J22	REXT_MPQ0	DGND	DGND	
J23	VSS	DGND	DGND	
J24	MPQ0_REFCLKP	MPQ_REF-CLK P0	FMC+ HPC	GBTCLK0_M2C_P
J25	MPQ0_REFCLKN	MPQ_REF-CLK N0	FMC+ HPC	GBTCLK0_M2C_N
J26	VSS	DGND	DGND	
K1	WRIO2_0A/SDQ0/UI/O	SPIM_DQ0	MX25L51245G	SI/SIO0
K2	VSS	DGND	DGND	
K3	VSS	DGND	DGND	
K4	VSS	DGND	DGND	
K5	WRIO2_3B/SDS/USI/O	LED2	RJ45	LED2_A
K6	VSS	DGND	DGND	
K7	VCCIO1	+3V3	PWR	+3V3
K8	VCCIO0	+3V3	PWR	+3V3
K9	VSS	DGND	DGND	

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
K10	VCCAUXA	VCCAUXA_1 V8	PWR	VCCAUXA_1V8
K11	VSS	DGND	DGND	
K12	VSS	DGND	DGND	
K13	VCCH_MPQ3	DGND	DGND	
K14	VSS	DGND	DGND	
K15	VSS	DGND	DGND	
K16	VCCH_MPQ2	DGND	DGND	
K17	VCC	+0V82	PWR	+0V82
K18	VSS	DGND	DGND	
K19	VSS	DGND	DGND	
K20	VCC	+0V82	PWR	+0V82
K21	VCCH_MPQ0	VCCH_MPQ0	PWR	VCCH_MPQ0
K22	VSS	DGND	DGND	
K23	HPIO11_2A/DP2_ DI/O	SW0	SW DIP-4	1
K24	VSS	DGND	DGND	
K25	VSS	DGND	DGND	
K26	HPIO11_13B/PLL CI/O	NC	NC	
L1	WRIO2_0B/SDQ1 /UI/O	SPIM_DQ1	MX25L51245G	SO/SIO1
L2	WRIO2_2B/SDQ3 /UI/O	SPIM_DQ3	MX25L51245G	RESET#/SIO3
L3	WRIO2_2A/SDQ2 /UI/O	SPIM_DQ2	MX25L51245G	WP#/SIO2
L4	VCCIO2	+3V3	PWR	+3V3
L5	WRIO2_3A/SCSN /UI/O	SPIM_CSN	MX25L51245G	CS#
L6	WRIO2_1B/SSDO	LED1	SN74AUP1G07DCK	A
L7	VCCA_PLL_W	VCCAPLL_0 V82	PWR	VCCAPLL_0V82
L8	VSS	DGND	DGND	
L9	WRIO0_1B/PCLK T0I/O	ETH0_RXCLK	KSZ9031RNX	RX_CLK/PHYAD2
L10	WRIO0_1A	ETH0_MDIO	KSZ9031RNX	MDIO
L11	WRIO0_3B/PCLK T0I/O	CLK50	ASDMB- 50.000MHZ-LC-T	OSC
L12	VCC_BAT	VCCBAT_1V 5 B	PWR	VCCBAT_1V5_B
L13	VSS	DGND	DGND	
L14	VCC	+0V82	PWR	+0V82
L15	VCC	+0V82	PWR	+0V82

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
L16	HPIO9_16A/DP2_DI/O	HA_P11	FMC+ HPC	HA11_P
L17	HPIO9_8A/DP2_DQI/O	HA_P2	FMC+ HPC	HA02_P
L18	HPIO9_0A/DP2_DQI/O	HA_P3	FMC+ HPC	HA03_P
L19	VCC	+0V82	PWR	+0V82
L20	VSS	DGND	DGND	
L21	HPIO11_14B/DP2_I/O	NC	NC	
L22	HPIO11_14A/DP2_I/O	NC	NC	
L23	HPIO11_2B/DP2_DI/O	SW1	SW DIP-4	2
L24	HPIO11_3A/DP2_DI/O	SW2	SW DIP-4	3
L25	HPIO11_3B/DP2_DI/O	SW3	SW DIP-4	4
L26	HPIO11_13A/PLL_TI/O	NC	NC	
M1	WRIO2_4B/SDQ5/UI/O	WDOGN	JP3	2
M2	WRIO2_4A/SDQ4/UI/O	ETH_RSTN	KSZ9031RNX	RESET_N
M3	TMS	TMS	FT4232H-56Q	BDBUS3
M4	TCK	TCK	FT4232H-56Q	BDBUS0
M5	INITN	INITN	+3V3	+3V3
M6	WRIO1_4B/MDQ5/UI/O	LED0	SN74AUP1G07DCK	A
M7	VCC	+0V82	PWR	+0V82
M8	VSS	DGND	DGND	
M9	VCC	+0V82	PWR	+0V82
M10	WRIO0_5A/UMCKOPI/O	ETH0_TX_CTL	KSZ9031RNX	TX_EN
M11	WRIO0_3A/UMCSN0I/O	ETH0_TXD3	KSZ9031RNX	TXD3
M12	VCC	+0V82	PWR	+0V82
M13	VSS	DGND	DGND	
M14	VSS	DGND	DGND	
M15	HPIO9_18B/DP2_DI/O	HA_N22	FMC+ HPC	HA22_N
M16	HPIO9_16B/DP2_DI/O	HA_N11	FMC+ HPC	HA11_N

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
M17	HPIO9_8B/DP2_D QI/O	HA_N2	FMC+ HPC	HA02_N
M18	HPIO9_0B/DP2_D QI/O	HA_N3	FMC+ HPC	HA03_N
M19	VSS	DGND	DGND	
M20	HPIO11_24A/PCL KI/O	NC	NC	
M21	HPIO11_12A/VRE FI/O	VREF11	VREF11	VREF11
M22	EXT_RES11/DP2_ EI/O	EXT_RES11	DGND	
M23	HPIO11_4A/DP2_ DI/O	NC	NC	
M24	HPIO11_4B/DP2_ DI/O	NC	NC	
M25	VSS	DGND	DGND	
M26	HPIO11_19A/DP2 I/O	DDR4_PAR	MT40A2G8AG	PAR
N1	PROGRAMN	PROGN	S2	S2
N2	VSS	DGND	DGND	
N3	VCCIO2	+3V3	PWR	+3V3
N4	WRIO2_5A/PCLK RTI/O	SPIM_SCK	MX25L51245G	SCLK
N5	WRIO1_6A/MDQ 6/UI/O	RXD1	FT4232H-56Q	DDBUS0
N6	WRIO1_4A/MDQ 4/UI/O	TXD1	FT4232H-56Q	DDBUS1
N7	VCCAUX	VCCAUX_1V 8	PWR	VCCAUX_1V8
N8	WRIO0_7B/PLLT FBI/O	ETH0_RX_C TL	KSZ9031RNX	RX_DV/CLK125_EN OUTPUT
N9	VCCIO0	+3V3	PWR	+3V3
N10	WRIO0_5B/UMC K0NI/O	ETH0_RXD0	KSZ9031RNX	RXD0/MODE0
N11	VCC	+0V82	PWR	+0V82
N12	VSS	DGND	DGND	
N13	VCC	+0V82	PWR	+0V82
N14	VSS	DGND	DGND	
N15	HPIO9_18A/DP2_ DI/O	HA_P22	FMC+ HPC	HA22_P
N16	VSS	DGND	DGND	
N17	VCCIO9	VBANK9	PWR	VADJ
N18	HPIO9_2B/DP2_D QI/O	HA_N13	FMC+ HPC	HA13_N

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
N19	VCC	+0V82	PWR	+0V82
N20	HPIO11_24B/PCL KI/O	DDR4_CAS	MT40A2G8AG	CAS_N/A15
N21	HPIO11_10B/PCL KI/O	NC	NC	
N22	VSS	DGND	DGND	
N23	HPIO11_6A/DP2_ DI/O	NC	NC	
N24	HPIO11_5B/DP2_ DI/O	NC	NC	
N25	VCCIO11	+1V2	DGND	+1V2
N26	HPIO11_19B/DP2 I/O	DDR4_BG1	MT40A2G8AG	BG1
P1	CFGMODE	CFGMODE	JP2	2
P2	TDI	TDI	FT4232H-56Q	BDBUS1
P3	TDO	TDO	FT4232H-56Q	BDBUS2
P4	DONE	DONE	LED	1
P5	VCCIO1	+3V3	PWR	+3V3
P6	WRIO1_6B/MDQ 7/UI/O	PG_M2C	FMC+ HPC	PG_M2C
P7	VSS	DGND	DGND	
P8	WRIO0_7A/PLLT 0 I/O	ETH0_RXD3	KSZ9031RNX	RXD3/MODE3
P9	WRIO0_4B/UMD Q0 I/O	ETH0_TXCLK	KSZ9031RNX	GTX_CLK
P10	WRIO0_4A/UMD Q0 I/O	ETH0_TXD2	KSZ9031RNX	TXD2
P11	VCC	+0V82	PWR	+0V82
P12	VSS	DGND	DGND	
P13	VCC	+0V82	PWR	+0V82
P14	VSS	DGND	DGND	
P15	HPIO9_20A/DP2_ DI/O	HA_P15	FMC+ HPC	HA15_P
P16	HPIO9_14A/DP2_ DI/O	HA_P19	FMC+ HPC	HA19_P
P17	HPIO9_12A/VRE F9I/O	VREF9	FMC+ HPC	VREF_A_M2C
P18	HPIO9_2A/DP2_D QI/O	HA_P13	FMC+ HPC	HA13_P
P19	VCC	+0V82	PWR	+0V82
P20	HPIO11_22B/DP2 I/O	NC	NC	
P21	HPIO11_10A/PCL KI/O	NC	NC	

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
P22	VCCIO11	+1V2	PWR	+1V2
P23	HPIO11_6B/DP2_DI/O	NC	NC	
P24	HPIO11_5A/DP2_DI/O	NC	NC	
P25	HPIO11_21A/DP2_I/O	DDR4_ACTN	MT40A2G8AG	ACT_N
P26	HPIO11_21B/DP2_I/O	DDR4_WE	MT40A2G8AG	WE_N/A14
R1	WRIO2_6A/SDQ6/UI/O	FMC_SDA	FMC+ HPC	SDA
R2	WRIO2_6B/SDQ7/UI/O	FMC_SCL	FMC+ HPC	SCL
R3	WRIO1_7B	FMC_PRSENT_N	FMC+ HPC	PRSENT_M2C_L
R4	WRIO1_7A/MRS_TN/I/O	RXD0	FT4232H-56Q	CDBUS0
R5	VSS	DGND	DGND	
R6	WRIO1_2A/MDQ2/UI/O	MSD2	MX25L51245G	WP#/SIO2
R7	VCC	+0V82	PWR	+0V82
R8	WRIO0_6A/UMDQ0_I/O	ETH0_RXD1	KSZ9031RNX	RXD1/MODE1
R9	VCCIO0	+3V3	PWR	+3V3
R10	VSS	DGND	DGND	
R11	VCC	+0V82	PWR	+0V82
R12	VCC	+0V82	PWR	+0V82
R13	VSS	DGND	DGND	
R14	VCC	+0V82	PWR	+0V82
R15	HPIO9_20B/DP2_DI/O	HA_N15	FMC+ HPC	HA15_N
R16	HPIO9_14B/DP2_DI/O	HA_N19	FMC+ HPC	HA19_N
R17	EXT_RES9/DP2_EXI/O	EXT_RES9	FMC+ HPC	VADJ
R18	HPIO9_4B/DP2_DQI/O	HA_N21	FMC+ HPC	HA21_N
R19	VSS	DGND	DGND	
R20	HPIO11_22A/DP2_I/O	NC	NC	
R21	HPIO11_8B/DP2_DI/O	NC	NC	
R22	VCCIO11	+1V2	DGND	+1V2

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
R23	HPIO11_7A/DP2_DI/O	NC	PWR	NC
R24	HPIO11_11A/PCLKI/O	NC	PWR	NC
R25	HPIO11_23B/DP2_I/O	DDR4_BA1	MT40A2G8AG	BA1
R26	HPIO11_23A/DP2_I/O	DDR4_BG0	MT40A2G8AG	BG0
T1	WRIO1_5A/MCLKP/I/O	MSCLK	MX25L51245G	SCLK
T2	WRIO1_3B/PCLKRTI/O	CLK100	ASDMB-100.000MHZ-XY-T	OSC
T3	VSS	DGND	DGND	
T4	VCCIO1	+3V3	PWR	+3V3
T5	WRIO1_2B/MDQ3/UI/O	MSD3	MX25L51245G	RESET#/SIO3
T6	VSS	DGND	DGND	
T7	VCC	+0V82	PWR	+0V82
T8	WRIO0_6B/UMDQ0 I/O	ETH0_RXD2	KSZ9031RNX	RXD2/MODE2
T9	VSS	DGND	DGND	
T10	WRIO0_0B/UMDQ0 I/O	ETH0_MDINT	KSZ9031RNX	INT_N
T11	VCC	+0V82	PWR	+0V82
T12	VSS	DGND	DGND	
T13	VCC	+0V82	PWR	+0V82
T14	VSS	DGND	DGND	
T15	HPIO9_22B/DP2_DI/O	HA_N20	FMC+ HPC	HA20_N
T16	HPIO9_10A/PCLKTI/O	HA_P14	FMC+ HPC	HA14_P
T17	HPIO9_10B/PCLKCI/O	HA_N14	FMC+ HPC	HA14_N
T18	HPIO9_4A/DP2_DQI/O	HA_P21	FMC+ HPC	HA21_P
T19	VCC	+0V82	PWR	+0V82
T20	HPIO11_20B/DP2_I/O	NC	NC	
T21	HPIO11_8A/DP2_DI/O	NC	NC	
T22	VSS	DGND	DGND	
T23	HPIO11_7B/DP2_DI/O	NC	NC	

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
T24	HPIO11_11B/PCLKI/O	NC	NC	
T25	VSS	DGND	DGND	
T26	HPIO10_2A/DP2_CI/O	DDR4_CKE	MT40A2G8AG	CKE
U1	WRIO1_5B/MCLKN/I/O	FMC_CLK_DIR	FMC+ HPC	CLK_DIR
U2	WRIO1_3A/MCSN/UI/O	MSCSN	MX25L51245G	CS#
U3	ERASEKEY	ERASEKEY	NC	
U4	WRIO1_1B/MSDO	TXD0	FT4232H-56Q	CDBUS1
U5	WRIO1_0A/MDQ0/UI/O	MSD0	MX25L51245G	SI/SIO0
U6	WRIO1_0B/MDQ1/UI/O	MSD1	MX25L51245G	SO/SIO1
U7	VCC	+0V82	PWR	+0V82
U8	WRIO0_2B/UMDQ0 I/O	ETH0_TXD1	KSZ9031RNX	TXD1
U9	WRIO0_2A/UMDQ0 I/O	ETH0_TXD0	KSZ9031RNX	TXD0
U10	WRIO0_0A/UMDQ0 I/O	ETH0_MDC	KSZ9031RNX	MDC
U11	VCCAUX	VCCAUX_1V8	PWR	VCCAUX_1V8
U12	VSS	DGND	DGND	
U13	VCCAUX	VCCAUX_1V8	PWR	VCCAUX_1V8
U14	VCCA_PLL7	VCCAPLL_0V82	PWR	VCCAPLL_0V82
U15	HPIO9_22A/DP2_DI/O	HA_P20	FMC+ HPC	HA20_P
U16	VCCIO9	VBANK9	FMC+ HPC	VADJ
U17	VCCA_PLL10	VCCAPLL_0V82	PWR	VCCAPLL_0V82
U18	VSS	DGND	DGND	
U19	VCCAUX	VCCAUX_1V8	PWR	VCCAUX_1V8
U20	HPIO11_20A/DP2_I/O	NC	NC	
U21	HPIO11_0B/DP2_DI/O	NC	NC	
U22	HPIO11_1A/DP2_DI/O	NC	NC	

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
U23	HPIO11_9A/DP2_DI/O	NC	NC	
U24	HPIO11_17B/DP2_I/O	NC	NC	
U25	VCCIO11	+1V2	MT40A2G8AG	VDD_1
U26	HPIO10_2B/DP2_MI/O	DDR4_A0	MT40A2G8AG	A0
V1	HPIO3_20B/DP0_DI/O	LA_N24	FMC+ HPC	LA24_N
V2	HPIO3_20A/DP0_DI/O	LA_P24	FMC+ HPC	LA24_P
V3	VSS	DGND	DGND	
V4	HPIO3_24B/PCLK_RI/O	LA_N17	FMC+ HPC	LA17_N_CC
V5	HPIO3_16B/DP0_DI/O	HB04_N	FMC+ HPC	HB04_N
V6	HPIO3_16A/DP0_DI/O	HB04_P	FMC+ HPC	HB04_P
V7	VSS	DGND	DGND	
V8	VCCA_PLL4	VCCAPLL_0V82	PWR	VCCAPLL_0V82
V9	HPIO3_2B/DP0_D_QI/O	LA_N13	FMC+ HPC	LA13_N
V10	HPIO3_2A/DP0_D_QI/O	LA_P13	FMC+ HPC	LA13_P
V11	HPIO3_0B/DP0_D_QI/O	LA_N10	FMC+ HPC	LA10_N
V12	VCC	+0V82	PWR	+0V82
V13	VSS	DGND	DGND	
V14	VCC	+0V82	PWR	+0V82
V15	HPIO9_24B/PCLK_RI/O	HA_N7	FMC+ HPC	HA07_N
V16	VSS	DGND	DGND	
V17	HPIO9_6B/DP2_D_QI/O	NC	NC	
V18	VCC	+0V82	PWR	+0V82
V19	HPIO11_18A/DP2_I/O	NC	NC	
V20	HPIO11_18B/DP2_I/O	NC	NC	
V21	HPIO11_0A/DP2_DI/O	NC	NC	
V22	HPIO11_1B/DP2_DI/O	LED3	SN74AUP1G07DCK	A

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
V23	HPIO11_9B/DP2_DI/O	NC	NC	
V24	HPIO11_17A/DP2_I/O	NC	NC	
V25	HPIO10_4A/DP2_MI/O	DDR4_A1	MT40A2G8AG	A1
V26	HPIO10_4B/DP2_MI/O	DDR4_A2	MT40A2G8AG	A2
W1	HPIO3_22B/DP0_DI/O	LA_N29	FMC+ HPC	LA29_N
W2	HPIO3_22A/DP0_DI/O	LA_P29	FMC+ HPC	LA29_P
W3	VCCIO3	VADJ	FMC+ HPC	VADJ
W4	HPIO3_24A/PCL_KRI/O	LA_P17	FMC+ HPC	LA17_P_CC
W5	HPIO3_14A/DP0_DI/O	HB00_P	FMC+ HPC	HB00_P_CC
W6	HPIO3_14B/DP0_DI/O	HB00_N	FMC+ HPC	HB00_N_CC
W7	VCCIO3	VADJ	FMC+ HPC	VADJ
W8	HPIO3_4A/DP0_D_QI/O	LA_P19	FMC+ HPC	LA19_P
W9	HPIO3_4B/DP0_D_QI/O	LA_N19	FMC+ HPC	LA19_N
W10	HPIO3_0A/DP0_D_QI/O	LA_P10	FMC+ HPC	LA10_P
W11	VSS	DGND	DGND	
W12	HPIO8_18B/DP1_DI/O	LA_N9	FMC+ HPC	LA09_N
W13	HPIO8_16A/DP1_DI/O	LA_P5	FMC+ HPC	LA05_P
W14	HPIO8_14A/DP1_DI/O	LA_P6	FMC+ HPC	LA06_P
W15	HPIO8_10B/PCLK_CI/O	CK_BD_N2	FMC+ HPC	CLK2_BIDIR_N
W16	HPIO9_24A/PCL_KRI/O	HA_P7	FMC+ HPC	HA07_P
W17	HPIO9_6A/DP2_D_QI/O	NC	NC	
W18	HPIO10_15A/DP2_I/O	DDR4_DQ10	MT40A2G8AG	DQ2
W19	HPIO11_16A/DP2_I/O	NC	NC	
W20	HPIO11_16B/DP2_I/O	NC	NC	

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
W21	HPIO11_15A/DP2 I/O	NC	NC	
W22	HPIO11_15B/DP2 I/O	NC	NC	
W23	HPIO10_0A/DP2_ MI/O	DDR4_CK_P	MT40A2G8AG	CK_T
W24	HPIO10_0B/DP2_ MI/O	DDR4_CK_N	MT40A2G8AG	CK_C
W25	HPIO10_8A/DP2_ MI/O	DDR4_A5	MT40A2G8AG	A5
W26	HPIO10_10A/PCL KI/O	DDR4_A7	MT40A2G8AG	A7
Y1	HPIO3_18B/DP0_ DI/O	LA_N28	FMC+ HPC	LA28_N
Y2	HPIO3_18A/DP0_ DI/O	LA_P28	FMC+ HPC	LA28_P
Y3	EXT_RES3/DP0_ EXI/O	EXT_RES3	DGND	
Y4	HPIO3_12A/VRE F3I/O	VREF3	FMC+ HPC	VREF_A_M2C
Y5	HPIO3_8A/DP0_D QI/O	NC	NC	
Y6	HPIO3_17A/DP0_ DI/O	LA_P26	FMC+ HPC	LA26_P
Y7	HPIO3_17B/DP0_ DI/O	LA_N26	FMC+ HPC	LA26_N
Y8	HPIO8_20A/DP1_ DI/O	LA_P14	FMC+ HPC	LA14_P
Y9	HPIO8_20B/DP1_ DI/O	LA_N14	FMC+ HPC	LA14_N
Y10	HPIO8_12A/VRE F8I/O	VREF8	FMC+ HPC	VREF_A_M2C
Y11	EXT_RES8/DP1_ EXI/O	EXT_RES8	DGND	
Y12	HPIO8_18A/DP1_ DI/O	LA_P9	FMC+ HPC	LA09_P
Y13	HPIO8_16B/DP1_ DI/O	LA_N5	FMC+ HPC	LA05_N
Y14	HPIO8_14B/DP1_ DI/O	LA_N6	FMC+ HPC	LA06_N
Y15	HPIO8_10A/PCL KTI/O	CK_BD_P2	FMC+ HPC	CLK2_BIDIR_P
Y16	HPIO9_15B/DP2_ DI/O	HA_N12	FMC+ HPC	HA12_N

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
Y17	HPIO9_15A/DP2_DI/O	HA_P12	FMC+ HPC	HA12_P
Y18	HPIO10_15B/DP2_I/O	DDR4_DQ14	MT40A2G8AG	DQ6
Y19	HPIO10_12A/VREFI/O	VREF10	VREF10	VREF10
Y20	HPIO11_25B/PCLKI/O	DDR4_RAS	MT40A2G8AG	RAS_N/A16
Y21	HPIO11_25A/PCLKI/O	DDR4_BA0	MT40A2G8AG	BA0
Y22	HPIO10_6A/DP2_MI/O	DDR4_A3	MT40A2G8AG	A3
Y23	HPIO10_6B/DP2_MI/O	DDR4_A4	MT40A2G8AG	A4
Y24	VCCIO10	+1V2	PWR	+1V2
Y25	HPIO10_8B/DP2_MI/O	DDR4_A6	MT40A2G8AG	A6
Y26	HPIO10_10B/PCLKI/O	DDR4_A8	MT40A2G8AG	A8
AA1	HPIO3_10B/PCLKCI/O	LA_N0	FMC+ HPC	LA00_N_CC
AA2	HPIO3_10A/PCLKTI/O	LA_P0	FMC+ HPC	LA00_P_CC
AA3	VSS	DGND	DGND	
AA4	VCCIO3	VADJ	PWR	VADJ
AA5	HPIO3_8B/DP0_DQI/O	Nc	NC	
AA6	HPIO3_11A/PCLKKTI/O	LA_P1	FMC+ HPC	LA01_P_CC
AA7	HPIO3_11B/PCLKCI/O	LA_N1	FMC+ HPC	LA01_N_CC
AA8	HPIO8_22B/DP1_DI/O	LA_N23	FMC+ HPC	LA23_N
AA9	HPIO8_8A/DP1_DQI/O	TXD_P	DS10BR150TSD/NO PB	IN-
AA10	HPIO8_8B/DP1_DQI/O	TXD_N	DS10BR150TSD/NO PB	IN+
AA11	HPIO8_6A/DP1_DQI/O	RXS_P	DS10BR150TSD/NO PB	OUT+
AA12	VSS	DGND	DGND	
AA13	VCCIO8	VADJ	PWR	VADJ
AA14	HPIO8_9B/DP1_DQI/O	TXS_N	DS10BR150TSD/NO PB	IN+
AA15	HPIO9_23A/DP2_DI/O	HA_P16	FMC+ HPC	HA16_P

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
AA16	VCCIO9	VBANK9	PWR	VADJ
AA17	VSS	DGND	DGND	
AA18	HPIO9_5A/DP2_D QI/O	HA_P8	FMC+ HPC	HA08_P
AA19	EXT_RES10/DP2_ EI/O	EXT_RES10	EXT_RES10	+1V2
AA20	VCCIO10	+1V2	PWR	+1V2
AA21	VSS	DGND	DGND	
AA22	HPIO10_18A/DP2 I/O	DDR4_DQS_ P0	MT40A2G8AG	DQS_T
AA23	HPIO10_16A/DP2 I/O	DDR4_DQ3	MT40A2G8AG	DQ3
AA24	VSS	DGND	DGND	
AA25	HPIO10_14B/DP2 I/O	DDR4_DQ1	MT40A2G8AG	DQ1
AA26	HPIO10_22A/DP2 I/O	DDR4_DQ2	MT40A2G8AG	DQ2
AB1	HPIO3_6A/DP0_D QI/O	LA_P31	FMC+ HPC	LA31_P
AB2	HPIO3_6B/DP0_D QI/O	LA_N31	FMC+ HPC	LA31_N
AB3	HPIO3_25A/PCL KRI/O	LA_P18	FMC+ HPC	LA18_P_CC
AB4	HPIO3_25B/PCLK RI/O	LA_N18	FMC+ HPC	LA18_N_CC
AB5	HPIO3_15A/DP0_ DI/O	HB06_P	FMC+ HPC	HB06_P_CC
AB6	HPIO3_15B/DP0_ DI/O	HB06_N	FMC+ HPC	HB06_N_CC
AB7	HPIO8_24B/PCLK RI/O	CK_M2C_N0	FMC+ HPC	CLK0_M2C_N
AB8	HPIO8_22A/DP1_ DI/O	LA_P23	FMC+ HPC	LA23_P
AB9	VCCIO8	VADJ	PWR	VADJ
AB10	VSS	DGND	DGND	
AB11	HPIO8_6B/DP1_D QI/O	RXS_N	DS10BR150TSD/NO PB	OUT-
AB12	HPIO8_21B/DP1_ WI/O	LA_N2	FMC+ HPC	LA02_N
AB13	HPIO8_21A/DP1_ MI/O	LA_P2	FMC+ HPC	LA02_P
AB14	HPIO8_9A/DP1_D QI/O	TXS_P	DS10BR150TSD/NO PB	IN-
AB15	HPIO9_23B/DP2_ DI/O	HA_N16	FMC+ HPC	HA16_N

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
AB16	HPIO9_17A/DP2_DI/O	HA_P17	FMC+ HPC	HA17_P_CC
AB17	HPIO9_11A/PCL_KTI/O	HA_P9	FMC+ HPC	HA09_P
AB18	HPIO9_5B/DP2_DQI/O	HA_N8	FMC+ HPC	HA08_N
AB19	VSS	DGND	DGND	
AB20	HPIO10_20B/DP2_I/O	DDR4_DQ7	MT40A2G8AG	DQ7
AB21	HPIO10_20A/DP2_I/O	DDR4_DQ5	MT40A2G8AG	DQ5
AB22	HPIO10_18B/DP2_I/O	DDR4_DQS_N0	MT40A2G8AG	DQS_C
AB23	HPIO10_16B/DP2_I/O	DDR4_DQ6	MT40A2G8AG	DQ6
AB24	HPIO10_14A/DP2_I/O	DDR4_DQ0	MT40A2G8AG	DQ0
AB25	HPIO10_1A/DP2_MI/O	NC	NC	
AB26	HPIO10_22B/DP2_I/O	DDR4_DQ4	MT40A2G8AG	DQ4
AC1	HPIO3_23A/DP0_DI/O	LA_P30	FMC+ HPC	LA30_P
AC2	HPIO3_23B/DP0_DI/O	LA_N30	FMC+ HPC	LA30_N
AC3	HPIO3_21B/DP0_DI/O	LA_N25	FMC+ HPC	LA25_N
AC4	HPIO3_21A/DP0_DI/O	LA_P25	FMC+ HPC	LA25_P
AC5	HPIO3_13A/PLLT3I/O	HB15_P	FMC+ HPC	HB15_P
AC6	HPIO3_13B/PLLC3I/O	HB15_N	FMC+ HPC	HB15_N
AC7	HPIO8_24A/PCL_KRI/O	CK_M2C_P0	FMC+ HPC	CLK0_M2C_P
AC8	HPIO8_2B/DP1_DQI/O	LA_N20	FMC+ HPC	LA20_N
AC9	HPIO8_25A/PCL_KRI/O	CK_M2C_P1	FMC+ HPC	CLK1_M2C_P
AC10	HPIO8_23A/DP1_BI/O	NC	NC	
AC11	HPIO8_19A/DP1_MI/O	LA_P8	FMC+ HPC	LA08_P
AC12	HPIO8_19B/DP1_MI/O	LA_N8	FMC+ HPC	LA08_N

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
AC13	HPIO8_13A/PLLT8I/O	NC	NC	
AC14	HPIO8_1A/DP1_DQI/O	LA_P16	FMC+ HPC	LA16_P
AC15	HPIO9_21B/DP2_DI/O	HA_N10	FMC+ HPC	HA10_N
AC16	HPIO9_17B/DP2_DI/O	HA_N17	FMC+ HPC	HA17_N_CC
AC17	HPIO9_11B/PCLKCI/O	HA_N9	FMC+ HPC	HA09_N
AC18	HPIO9_7A/DP2_DQI/O	HA_P6	FMC+ HPC	HA06_P
AC19	HPIO10_25A/PCLKI/O	DDR4_DM1	MT40A2G8AG	DM_N/DBI_N/TDQSPASSIVE
AC20	HPIO10_21A/DP2I/O	DDR4_DQ15	MT40A2G8AG	DQ7
AC21	VSS	DGND	DGND	
AC22	HPIO10_7A/DP2_CI/O	DDR4_CS	MT40A2G8AG	CS_N
AC23	HPIO10_5A/DP2_OI/O	DDR4_ODT	MT40A2G8AG	ODT
AC24	VSS	DGND	DGND	
AC25	HPIO10_1B/DP2_MI/O	NC	NC	
AC26	HPIO10_24A/PCLKI/O	DDR4_DM0	MT40A2G8AG	DM_N/DBI_N/TDQSPASSIVE
AD1	HPIO3_19A/DP0_DI/O	LA_P33	FMC+ HPC	LA33_P
AD2	HPIO3_19B/DP0_DI/O	LA_N33	FMC+ HPC	LA33_N
AD3	VSS	DGND	DGND	
AD4	HPIO3_9B/DP0_DQI/O	HB17_N	FMC+ HPC	HB17_N_CC
AD5	HPIO3_9A/DP0_DQI/O	HB17_P	FMC+ HPC	HB17_P_CC
AD6	HPIO8_4B/DP1_DQI/O	LA_N22	FMC+ HPC	LA22_N
AD7	HPIO8_4A/DP1_DQI/O	LA_P22	FMC+ HPC	LA22_P
AD8	HPIO8_2A/DP1_DQI/O	LA_P20	FMC+ HPC	LA20_P
AD9	HPIO8_25B/PCLKRI/O	CK_M2C_N1	FMC+ HPC	CLK1_M2C_N
AD10	HPIO8_23B/DP1_BI/O	NC	NC	

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
AD11	VCCIO8	VADJ	PWR	VADJ
AD12	VSS	DGND	DGND	
AD13	HPIO8_13B/PLLC 8I/O	NC	NC	
AD14	HPIO8_1B/DP1_D QI/O	LA_N16	FMC+ HPC	LA16_N
AD15	HPIO9_21A/DP2_ DI/O	HA_P10	FMC+ HPC	HA10_P
AD16	VCCIO9	VBANK9	FMC+ HPC	VADJ
AD17	VSS	DGND	DGND	
AD18	HPIO9_7B/DP2_D QI/O	HA_N6	FMC+ HPC	HA06_N
AD19	HPIO10_25B/PCL KI/O	DDR4_RE- SETN	MT40A2G8AG	RESET_N
AD20	HPIO10_21B/DP2 I/O	DDR4_DQ11	MT40A2G8AG	DQ3
AD21	VCCIO10	+1V2	PWR	+1V2
AD22	HPIO10_7B/DP2_ MI/O	DDR4_A9	MT40A2G8AG	A9
AD23	HPIO10_5B/DP2_ CI/O	NC	NC	
AD24	VCCIO10	+1V2	PWR	+1V2
AD25	HPIO10_3A/DP2_ CI/O	NC	NC	
AD26	HPIO10_24B/PCL KI/O	DDR4_ALER TN	MT40A2G8AG	ALERT_N
AE1	HPIO3_7B/DP0_D QI/O	LA_N32	FMC+ HPC	LA32_N
AE2	HPIO3_7A/DP0_D QI/O	LA_P32	FMC+ HPC	LA32_P
AE3	VCCIO3	VADJ	PWR	VADJ
AE4	HPIO3_3A/DP0_D QI/O	LA_P27	FMC+ HPC	LA27_P
AE5	HPIO3_3B/DP0_D QI/O	LA_N27	FMC+ HPC	LA27_N
AE6	HPIO8_0A/DP1_D QI/O	LA_P21	FMC+ HPC	LA21_P
AE7	HPIO8_0B/DP1_D QI/O	LA_N21	FMC+ HPC	LA21_N
AE8	VSS	DGND	DGND	
AE9	VCCIO8	VADJ	PWR	VADJ
AE10	HPIO8_11A/PCL KTI/O	CK_BD_P3	FMC+ HPC	CLK3_BIDIR_P

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
AE11	HPIO8_7B/DP1_D QI/O	RXD_N	DS10BR150TSD/NO PB	OUT-
AE12	HPIO8_5A/DP1_D QI/O	LA_P4	FMC+ HPC	LA04_P
AE13	HPIO8_3A/DP1_D QI/O	LA_P3	FMC+ HPC	LA03_P
AE14	HPIO9_25A/PCL KRI/O	HA_P1	FMC+ HPC	HA01_P_CC
AE15	HPIO9_19A/DP2_ DI/O	HA_P18	FMC+ HPC	HA18_P
AE16	HPIO9_13A/PLLT 9I/O	HA_P23	FMC+ HPC	HA23_P
AE17	HPIO9_9A/DP2_D QI/O	HA_P4	FMC+ HPC	HA04_P
AE18	HPIO9_3A/DP2_D QI/O	HA_P5	FMC+ HPC	HA05_P
AE19	HPIO9_1A/DP2_D QI/O	HA_P0	FMC+ HPC	HA00_P_CC
AE20	HPIO10_23A/DP2 I/O	DDR4_DQ12	MT40A2G8AG	DQ4
AE21	HPIO10_19A/DP2 I/O	DDR4_DQS_ P1	MT40A2G8AG	DQS_T
AE22	HPIO10_17A/DP2 I/O	DDR4_DQ9	MT40A2G8AG	DQ1
AE23	HPIO10_13A/PLL TI/O	DDRCLK_P	AX3DAF1- 100.0000T LVDS	CLK_N
AE24	HPIO10_11A/PCL KI/O	DDR4_A12	MT40A2G8AG	A12/BC_N
AE25	HPIO10_9A/DP2_ MI/O	DDR4_A10	MT40A2G8AG	A10/AP
AE26	HPIO10_3B/DP2_ OI/O	NC	NC	
AF1	VSS	DGND	DGND	
AF2	HPIO3_5A/DP0_D QI/O	LA_P15	FMC+ HPC	LA15_P
AF3	HPIO3_5B/DP0_D QI/O	LA_N15	FMC+ HPC	LA15_N
AF4	HPIO3_1B/DP0_D QI/O	LA_N11	FMC+ HPC	LA11_N
AF5	HPIO3_1A/DP0_D QI/O	LA_P11	FMC+ HPC	LA11_P
AF6	HPIO8_17A/DP1_ MI/O	LA_P12	FMC+ HPC	LA12_P
AF7	HPIO8_17B/DP1_ MI/O	LA_N12	FMC+ HPC	LA12_N

FPGA pin	FPGA pin name	Net name	End component	End Pin Name
AF8	HPIO8_15B/DP1_MI/O	LA_N7	FMC+ HPC	LA07_N
AF9	HPIO8_15A/DP1_MI/O	LA_P7	FMC+ HPC	LA07_P
AF10	HPIO8_11B/PCLK CI/O	CK_BD_N3	FMC+ HPC	CLK3_BIDIR_N
AF11	HPIO8_7A/DP1_D QI/O	RXD_P	DS10BR150TSD/NO PB	OUT+
AF12	HPIO8_5B/DP1_D QI/O	LA_N4	FMC+ HPC	LA04_N
AF13	HPIO8_3B/DP1_D QI/O	LA_N3	FMC+ HPC	LA03_N
AF14	HPIO9_25B/PCLK RI/O	HA_N1	FMC+ HPC	HA01_N_CC
AF15	HPIO9_19B/DP2_DI/O	HA_N18	FMC+ HPC	HA18_N
AF16	HPIO9_13B/PLL CI/O	HA_N23	FMC+ HPC	HA23_N
AF17	HPIO9_9B/DP2_D QI/O	HA_N4	FMC+ HPC	HA04_N
AF18	HPIO9_3B/DP2_D QI/O	HA_N5	FMC+ HPC	HA05_N
AF19	HPIO9_1B/DP2_D QI/O	HA_N0	FMC+ HPC	HA00_N_CC
AF20	HPIO10_23B/DP2 I/O	DDR4_DQ8	MT40A2G8AG	DQ0
AF21	HPIO10_19B/DP2 I/O	DDR4_DQS_N1	MT40A2G8AG	DQS_C
AF22	HPIO10_17B/DP2 I/O	DDR4_DQ13	MT40A2G8AG	DQ5
AF23	HPIO10_13B/PLL CI/O	DDRCLK_N	AX3DAF1-100.0000T LVDS	CLK_P
AF24	HPIO10_11B/PCLKI/O	DDR4_A13	MT40A2G8AG	A13
AF25	HPIO10_9B/DP2_MI/O	DDR4_A11	MT40A2G8AG	A11
AF26	VSS	DGND	DGND	

## **APPENDIX C – BOARD SCHEMATIC**

The schematic file [RD1] is provided only upon the procurement of the board.

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