GR718-BOARD

Development Board

2018 User's Manual

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GR718-BOARD

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User's Manual

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1 Introduction

1.1 Overview

This document describes the *GR718-BOARD* Development Board.

The purpose of this equipment is to provide developers with a convenient hardware platform for the evaluation and development of software for the *Cobham Gaisler GR718B Radiation-Tolerant 18x SpaceWire Router.*

The GR718B Radiation-Tolerant 18x SpaceWire Router implements a routing switch as defined in the ECSS-E-ST-50-12C Rev 1 SpaceWire links, nodes, routers and networks standard, supporting all mandatory and optional features.

The *GR718-BOARD* Development Board comprises a custom designed PCB in a 6U Compact PCI format, making the board suitable for stand-alone bench top development, or if required, to be mounted in a 6U CPCI Rack.

The principle interfaces and functions are accessible on the front and back edges of the board, and secondary interfaces via headers on the board.

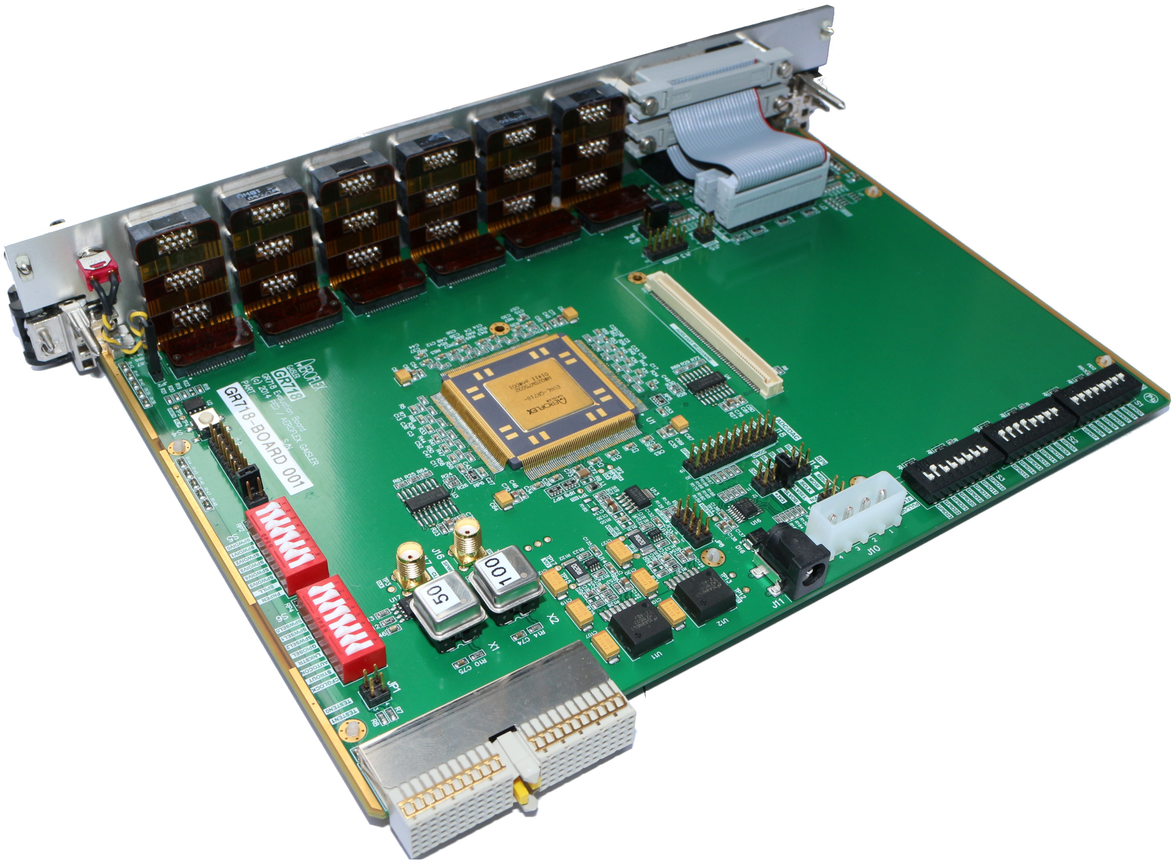

Figure 1-1: GR718-BOARD Development Board

The board contains the following main items as detailed in section 2 of this document:

- GR718B 18-x SPW Router ASIC in CQFP-256 package,
  operating with a frequency of 50MHz.
- Sixteen SPW (LVDS) interfaces with front-panel MDM9S connectors
- Two SPW interfaces with on-board LVDS transceivers and front-panel MDM9S connectors
- 24 General Purpose I/O signals on headers which are connected to the front panel
- Octal SPDT DIP Switches for configurable Pull-up/Pull-down of the GPIO pins to allow a configurable power-on pin-strapping to be implemented
- 24 front panel LED's indicating the high/low state of the multi-function GPIO pins
- 2 front panel LED's indicating the 'power' status
- 2 front panel LED's indicating the "irq' and 'lock' status
- One FTDI USB interface (with a USB Mini-AB connector) providing two serial links, one for JTAG Debug Link, and one for Console UART connections to the ASIC
- Front panel RESET push-button
- SPST DIP switches for ASIC configuration pins
- Compact PCI connector to provide input power (+5V) when connected in a CPCI backplane
- On-Board power circuits for 3.3V, 1.8V and Vcore for FPGA, generated from +5V input.
- Miscellaneous support components for clock, reset, indicators and bootstrap signals

Additionally, a mezzanine connector is provided to provide access to the status and control signals of the ASIC, and to enable a user defined mezzanine to be implemented.

To enable convenient connection to the interfaces, most connector types and pin-outs are compatible with the standard connector types for these types of interfaces.

1.2 References

RD-1	GR718-BOARD_schematic.pdf, Schematic (included on CD)
RD-2	GR718-BOARD_assy_drawing.pdf, Assembly Drawing (included on CD)
RD-3	GR718-BOARD_bom.pdf, Bill of Materials (included in CD)
RD-4	GR718B Advanced Data Sheet and User's Manual, Cobham Gaisler
RD-5	GRMON2 User Manual, Cobham Gaisler, part of GRMON2 package.
RD-6	GR-MEZZ Technical Note, Technical Note about Mezzanine connectors

1.3 Handling

ATTENTION : OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES

This unit contains sensitive electronic components which can be damaged by Electrostatic Discharges (ESD). When handling or installing the unit observe appropriate precautions and ESD safe practices.

When not in use, store the unit in an electrostatic protective container or bag.

When configuring the jumpers on the board, or connecting/disconnecting cables, ensure that the unit is in an un-powered state.

When operating the board in a 'stand-alone' configuration, the power supply should be current limited to prevent damage to the board or power supply in the event of an over-current situation.

This board is intended for commercial use and evaluation in a standard laboratory environment, nominally, 20°C. All devices are standard commercial types, intended for use over the standard commercial operating temperature range (0 to 70°C).

1.4 Abbreviations

ASIC	Application Specific Integrated Circuit.
CPCI	Compact Peripheral Connect Interface
DIL	Dual In-Line
DSU	Debug Support Unit
ESD	Electro-Static Discharge
GPIO	General Purpose Input / Output
I/O	Input/Output
IP	Intellectual Property
PCB	Printed Circuit Board
SPDT	Single Pole Double Throw
SPW	Spacewire
TBC	To be Confirmed

2 Electrical Design

2.1 GR718B ASIC

The Cobham Gaisler GR718B 18x SpaceWire Router ASIC consists of multiple SPW ports linked with an internal switch matrix. Additionally the device has a set of IP cores for GPIO, UART, SPI and JTAG functions, connected through AMBA AHB/APB buses as represented in Figure 2-1, and as defined in detail in RD-4.

The GR718B is packaged in a 256 pin, 0.5 mm pitch Ceramic Flat pack (35 x 35 mm), and is soldered on to the PCB. For more details see RD-4.

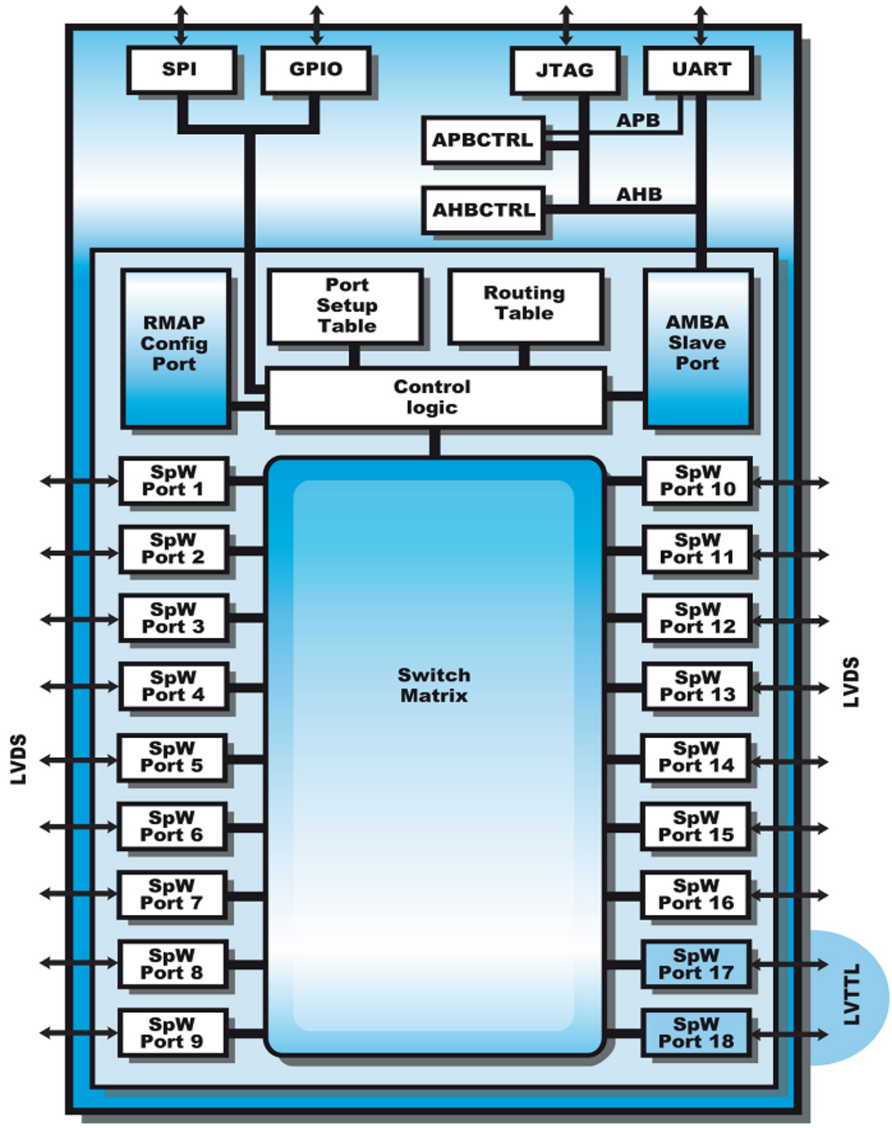

Figure 2-1: GR718B SOC Block Diagram

The details of the interfaces, operation and programming of the GR718 ASIC is given in the GR718B Advanced Data Sheet and User's Manual, RD-4.

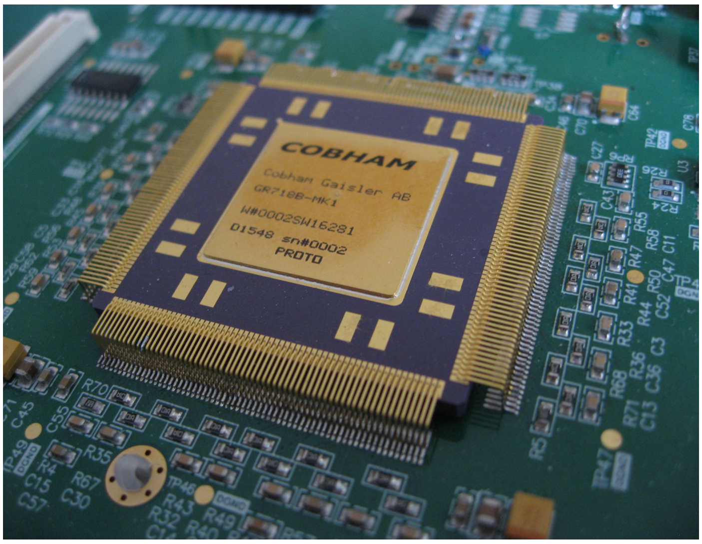

Figure 2-2: GR718B-ASIC

2.2 Board Block Diagram

The *GR718-BOARD* Board provides the electrical functions and interfaces as represented in the block diagram, Figure 2-3.

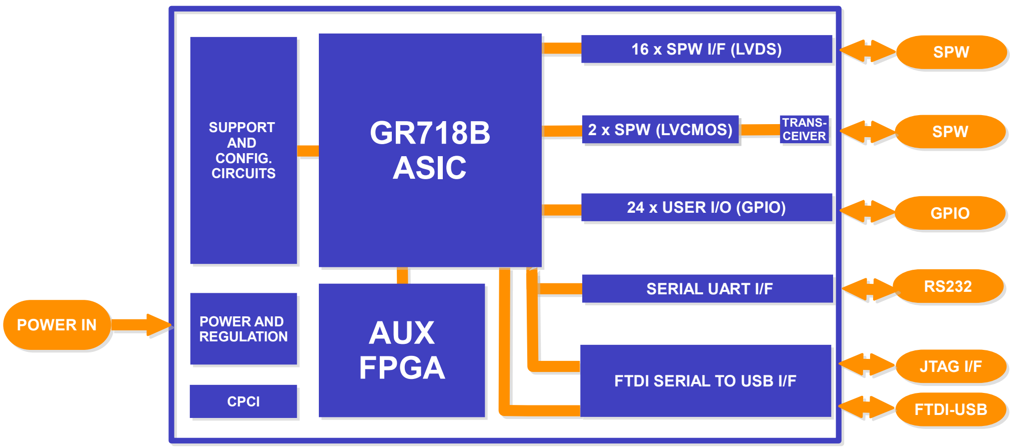

Figure 2-3: Block Diagram of GR718-BOARD board

2.3 Board Mechanical Configuration

The Main PCB is a 6U Compact PCI format board (233.5 x 160mm) and can be used 'stand-alone' on the bench-top simply using an external +5V power supply, or can be plugged in to a Compact PCI backplane.

Figure 1-1, shows the board as a stand alone PCB. However, for installation into a Compact PCI rack, this board is provided with a custom CPCI front panel with the with the appropriate connector cut-outs. The front panel concept is shown in Figure 2-4, with MDM9S style connectors for the Spacewire interfaces.

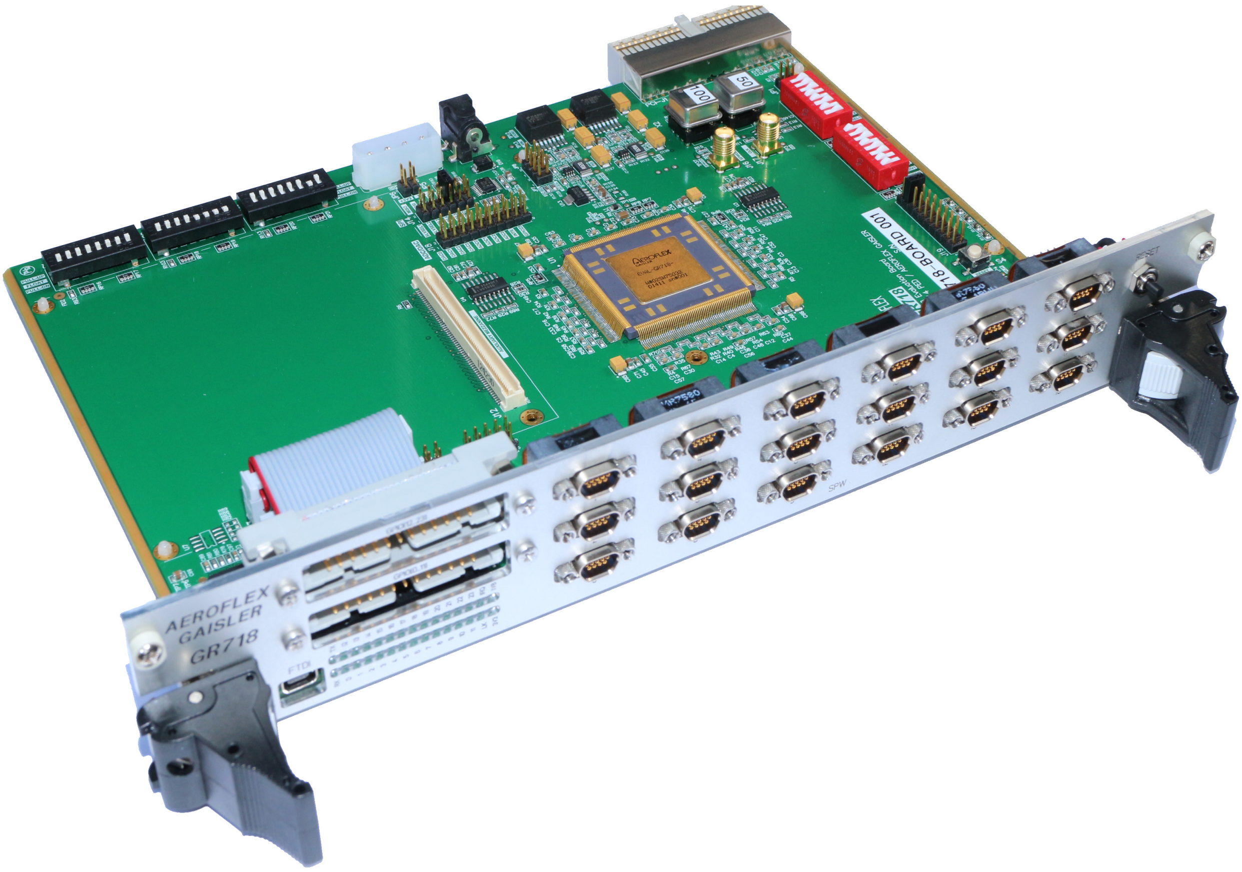

Figure 2-4: GR718-BOARD Board with CPCI Front Panel

Additionally, the board concept is compatible with its installation in a housing. This configuration requires the housing itself, and the replacement of the CPCI front panel with a custom front panel to suit the housing. The advantage of the housing is that it provides a robust and protected environment for the board, which would be suitable to allow its use in a desktop environment, for example during software development or evaluation. The disadvantage of the housing is that it restricts the access to some of the configuration features of the board (DIP switches or jumpers) and therefore may hinder the easy use of some of the features.

2.4 GR718 Router

2.4.1 Spacewire Interfaces

The *GR718B* ASIC provides 18 Spacewire interfaces. 16 of these interfaces have LVDS signal levels at the ASIC pins and are routed directly to the front panel of the board. The remaining two interfaces have LVCMOS voltage levels (3.3V) which require transceiver circuits to convert to the required LVDS levels at the front panel.

Each Spacewire interface consists of 4 LVDS differential pairs (2 input pairs and 2 output pairs).

The PCB traces for the LVDS signals on the *GR718-BOARD* board are laid out with 100-Ohm differential impedance design rules and, within groups of signals, matched trace lengths.

100 Ohm Termination resistors for the LVDS receiver signals are mounted on the board close to the receiver pins, and an effort has been made to minimise stubs or discontinuities in the routing paths.

The ASIC and board support a link rate for Spacewire up to 200 Mbit/s.

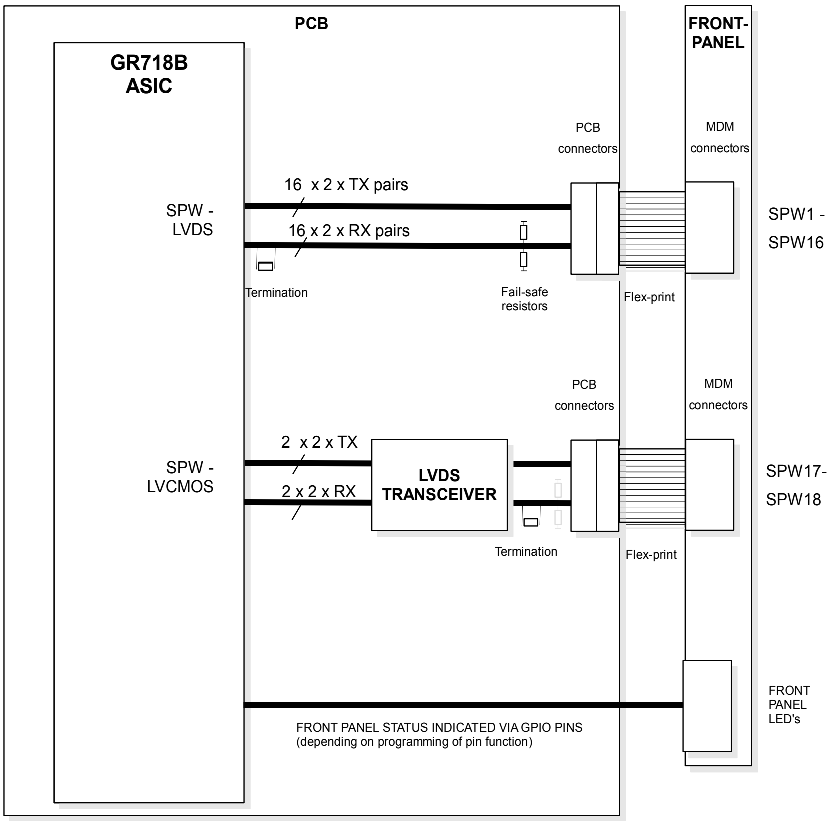

Figure 2-5: SPW interface

2.4.2 SPW Connectors

In order to be compatible with other SPW equipment, standard MDM9S connectors are mounted on the CPCI front panel for the Spacewire interfaces. The pin out of the MDM9S connectors for these Spacewire interfaces conform to the Spacewire standard. In order to make the transition from the PCB to the front panel, 40 pin high speed SAMTEC connectors together with a small flex-prints are used, as shown in Figure 2-6.

Figure 2-6: SPW flex connection

2.4.3 Serial Interface (RS232)

The *GR718B ASIC* has one serial port with TXD/RXD pins. The *GR718-BOARD* board provides an RS232 interface circuit and a 10 pin header on board.

The RS232 transceiver IC on this board is a SN75C3232 device from Texas Instruments which operates from a single +3.3V power supply.

The layout and pin ordering of the 10 pin header is designed so that a simple 1-to-1 ribbon cable connection can be made to a 'standard' Female D-Sub 9 pin type connector with a standard pin-out for serial links.

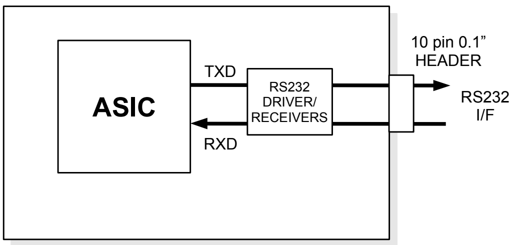

Figure 2-7: Serial interface

Note: As explained in the following section, the serial interfaces of the *GR718* can either be connected to these pin-headers (RS232) or to the FTDI-USB interface chip, depending on the setting of the jumpers *JP3* and *JP4.* The user should take care to set the appropriate jumper configuration depending on the configuration required.

2.4.4 FTDI Serial to USB Interface

To provide additional flexibility, an FTDI *FT2232HL* Serial to USB interface chip is provided on board.

This device provides two Ports which connect to a single Mini-AB USB connector (*J1*) on the front panel. This USB port can be connected to a host computer to allow communication over serial interfaces to Host PC's which do not have conventional 9 pin D-sub type RS232 connectors.

Additionally, the FTDI *FT2232HL* chip is also able to perform a JTAG to USB conversion function. This functionality is supported by the latest versions of the *GRMON* debug software, allowing debugging via the JTAG interface to be performed without requiring a special JTAG cable.

As represented in Figure 2-8, sets of jumpers allow a number of possibilities to be configured:

1. Connect UART to RS232 header J13 (JP3 position 1-3 and 2-4)
2. Connect UART to FTDI port B (JP3 position 3-5 and 4-6)
3. Connect I2C signals to FTDI port B (JP3 position 5-7 and 6-8 and JP4 1-2)
4. Connect JTAG-DSU to FTDI port A (no configuration required)

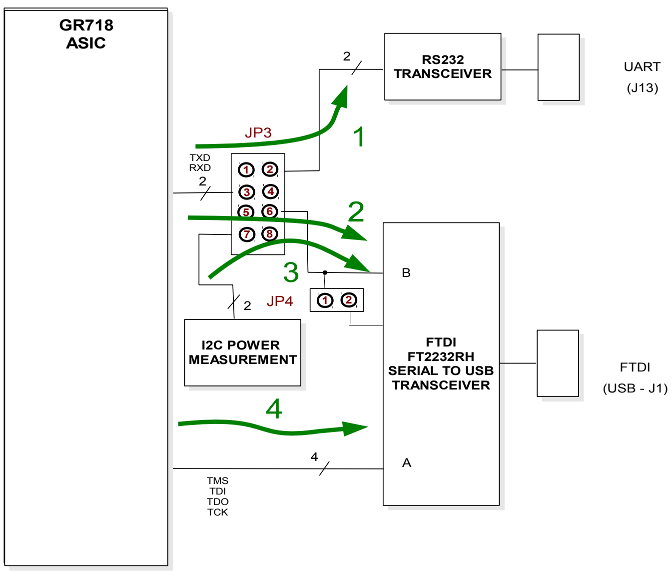

Figure 2-8: Block diagram of FTDI Serial/JTAG to USB Interface

2.4.5 SPI interface

The *GR718B ASIC* provides an SPI interface for user defined devices. The *GR718B* SPI controller always acts as a *Master,* and can address up to 6 slave devices.

As shown in Figure 2-9, the SPI interface pins of the *GR718B ASIC* are connected to a 12 pin 0.1” header on the board (*J14*) to allow external SPI circuits to be hooked-up.

Additionally, as an example SPI circuit, the *GR718-BOARD* Board provides an *AD7516*, 'SPI/I^{2}C Compatible, Temperature Sensor, 4-Channel ADC and Quad Voltage Output Temperature monitor circuit' on the board.

By configuring the jumper *J14*, the chip-select pin of the ADC/DAC can be set to either use *SLVSEL* (insert jumper *J14 pins 8-10*) or to use *SLVSEL5* (insert jumper *J14 pins 9-10*).

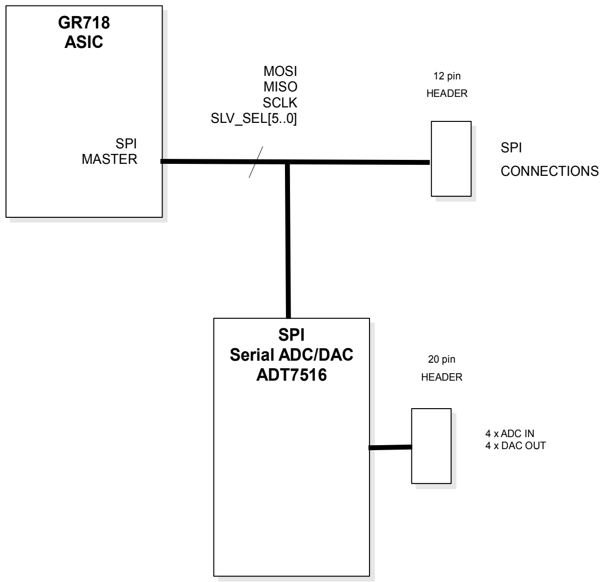

Figure 2-9: SPI Interface Configuration

The *ADT7516* provides four 12 bit DAC outputs and four 10 bit ADC inputs.

A 20 pin header, *J18*, is provided on the board to allow user access to these signals.

Additionally, the *ADT7516* also provides an internal temperature reference sensor and ADC channel dedicated to monitoring its power supply rail (+3.3V).

Please note that, if using the 20 pin header signals, the user must pay attention to the voltage range being applied, and if necessary must scale it appropriately, for example with a resistor divider or filter. The input voltage should not exceed the supply voltage of 3.3V. However, the full-scale input range of the ADC may be lower than this depending on the reference voltage and the internal gain/scale factor which has been programmed.

Please refer to the datasheet for the *ADT7516* for more information on its functions, internal registers and programming.

2.4.6 GPIO

The *GR718B ASIC* provides 24 general Purpose Input Output signals (3.3V LVCMOS voltage levels).

These 24 signals are multi-functional, depending on how internal registers are programmed within the device. Please refer to *RD-4* for more information on the functions of these pins.

On the *GR718-BOARD*, each GPIO pin is connected to the following circuits as represented in Figure 2-10.

- to a double-throw switch which allows the pin to 'float', 'pull-up to +3V3' or 'pull-down to DGND'.
- connected to a header on the board to allow easy access for measurement This header, in turn can be connected with a short ribbon cable to a corresponding header on the front panel (Figure 2-11). A series protection resistor of 470 Ohm is included on each signal to provide a simple level of protection in the case of a short circuit at the front panel
- connected to a front panel LED (via a driver) to indicate the state of the pin at the ASIC
- connected to a mezzanine connector to allow an external user-defined circuit to monitor GPIO output state or to or drive the GPIO input state.

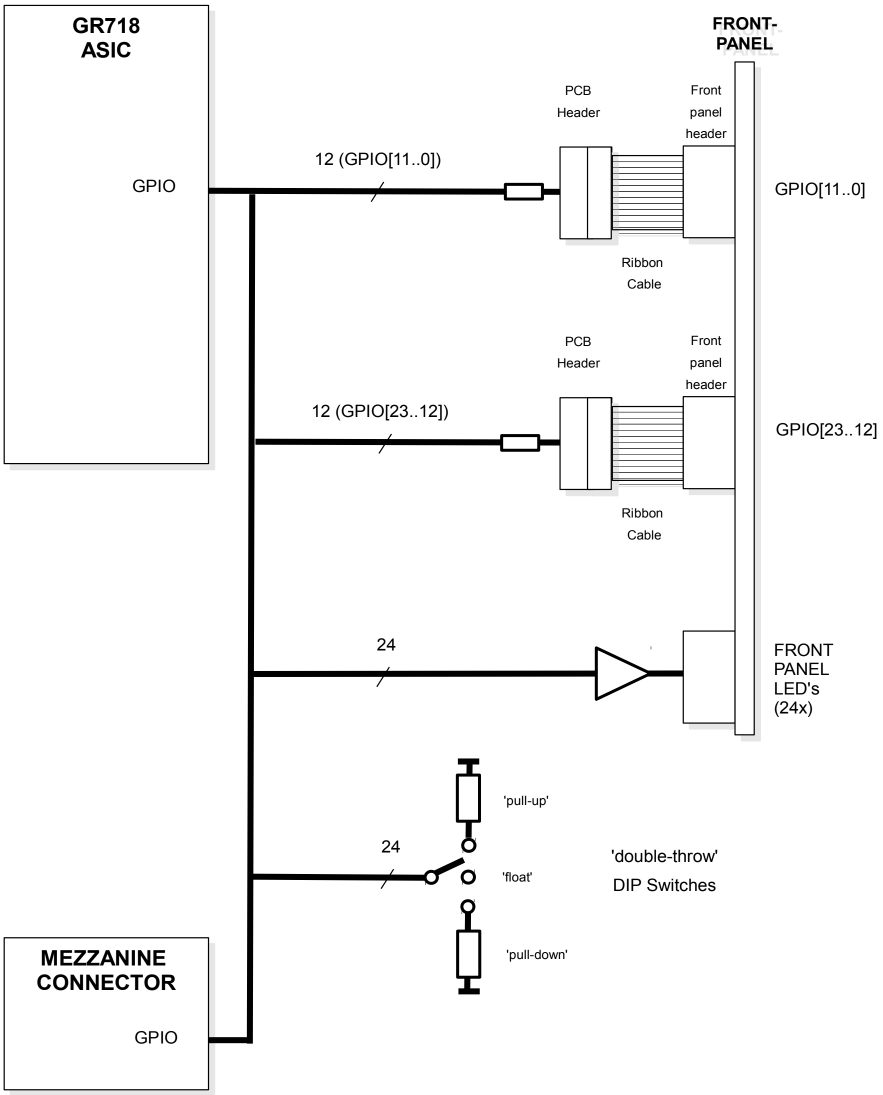

Figure 2-10: GPIO interface configuration

Note that the state of the GPIO[23..16] pins is sampled at power-up or reset of the processor in order to determine initial conditions of a number of internal features. Please refer to section 2.7 ('GPIO pin Multiplexing') of RD-4.

To ensure the correct initialisation of the processor, the user should ensure that the initial DIP switch settings are correctly set to set the users' required configuration at power up or reset of the board. After reset, the GPIOs can be used as normal I/Os.

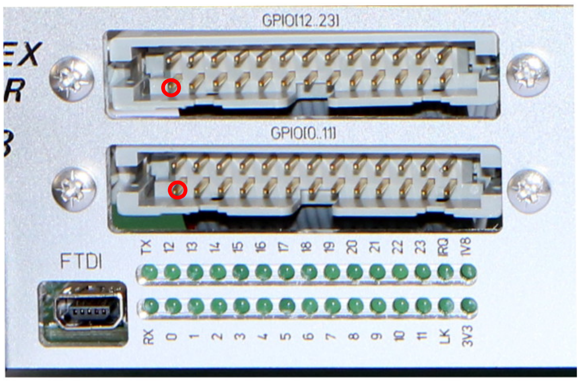

Figure 2-11: Front Panel GPIO connections

(pin 1 marked with red circle)

Additionally, two 8 pole DIP switches, S5 and S6, are provided to allow the user to conveniently set the state of the ASIC control pins as listed in the tables below: For more information on the function of these pins, refer to section 2.4 ('I/O Pins') of RD-4.

When the switch is 'open' a pull-up resistor will pull the pin to 3.3V (= logic '1'). When the switch is 'closed', the pin will be connected to DGND (= logic '0').

SWITCH	Function	Comment
1	SPWCLKDIV0	Reset value for bit 0 of the SpaceWire port’s clock divisor register
2	SPWCLKDIV1	Reset value for bit 1 of the SpaceWire port’s clock divisor register
3	SPWCLKDIV2	Reset value for bit 2 of the SpaceWire port’s clock divisor register
4	SPWCLKDIV3	Reset value for bit 3 of the SpaceWire port’s clock divisor register
5	SPWCLKDIV4	Reset value for bit 4 of the SpaceWire port’s clock divisor register
6	SPWCLKDIV5	Reset value for bit 5 of the SpaceWire port’s clock divisor register
7	SPILL	Sets the reset value for the SPILL-IF-NOT-READY feature
8	PNPEN	Enables / disables SpaceWire Plug-and-Play at reset

Table 1: DIP Switch S5 Definitions

SWITCH	Function	Comment
1	SPWCLKSEL0	Selects internal SpaceWire clock, bit 0
2	SPWCLKSEL1	Selects internal SpaceWire clock, bit 1
3	SPWCLKSEL2	Selects internal SpaceWire clock, bit 2
4	GPIOSEL	Selects the function of the GPIO[23:0] pins
5	LNKSTR	Reset value for the SpaceWire ports' link-start-on-request feature.
6	AUTOCON	Reset value for the SpaceWire ports' auto-disconnect feature.
7	STROUT	Enables / disables the static routing feature at reset
8	CFGLOCK	Locks config port (port 0) from accesses from all ports except 1 and 2.

Table 2: DIP Switch S6 Definitions

2.4.7 Debug Support Unit Interface (JTAG)

Debug monitoring of the *GR718B* ASIC can be performed using the GRMON Debug Monitor tool from Cobham Gaisler (RD-5). The *GR718 ASIC* provides a JTAG interface for Debug and control of the processor by means of a host terminal via its DSU interface, as represented in Figure 2-12. As has been described in section 2.4.4, this connection is achieved via the front-panel USB connector and the FTDI interface circuitry.

Note that the JTAG signals (TMS, TCK, TDI, TDO) from the GR718 ASIC are also connected to pins on the auxiliary mezzanine connector to potentially allow a circuit on the mezzanine to be connected to the same JTAG chain as the DSU-JTAG. However, in the default case, the resistor shown 'dotted' in the figure is installed so that the TDO-TDI signal chain ignores the mezzanine.

If the mezzanine requires to be included in the JTAG chain, then this resistor should be removed to allow the correct flow of the TDO-TDI signal chain.

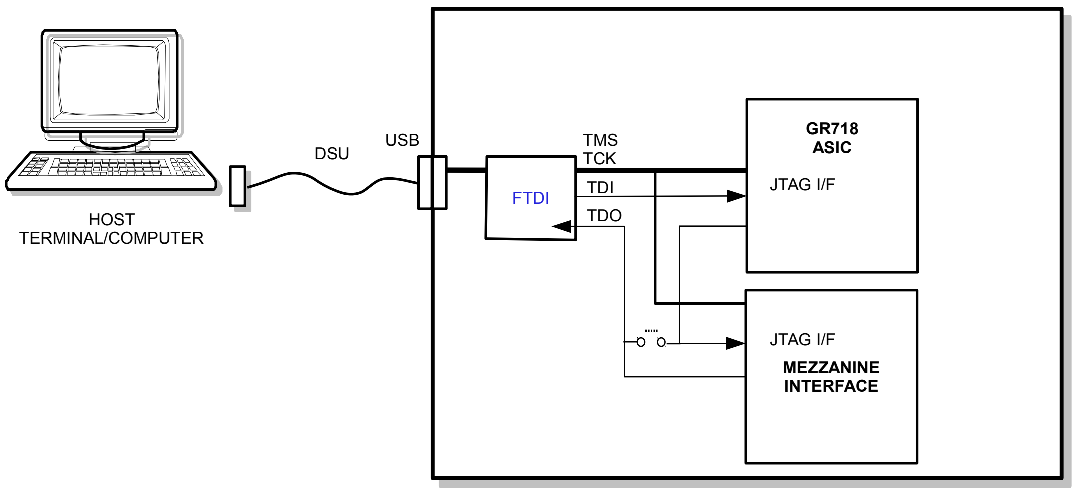

Figure 2-12: Debug Support Unit connections

2.5 Auxiliary Mezzanine

The board implements a Mezzanine connector, allowing user-designed logic to be implemented on a mezzanine board.

The following signals to/from the GR718B ASIC are connected to the Mezzanine connector

GPIO[23..0]
SPWCLKDIV[5..0]
SPWCLKSEL[2..0]
SPILL
PNPEN
TESTEN[1..0]
GPIOSEL
LNKSTREQ
AUTOCONN
STROUTEEN
CFGLOCK
TCK
TMS
TDF (TDI to mezzanine)
TDO
SPI_MISO
SPI_MOSI
SPI_SLVSEL
SPI_SCK
AUXTICKIN
AUXTICKOUT
IRQ
LOCK
RESETN
CLK

Table 3: FPGA Signals

Note that many of these signals are connected to elsewhere on the board (e.g. DIP switches or front panel headers), and this should be taken account to ensure that there is not a conflict between the circuits implemented on the mezzanine board and any other source which may be driving the signal.

Please note that this pin ordering as used on this board does not match exactly the pin ordering which you will find on the Tyco part datasheets for the Mezzanine board mating connectors. The reason for this is explained in more detail in the Technical Note, RD-6

Therefore please take care when designing your own mezzanine boards to take account of this pin ordering.

If there is any confusion, or you have any doubts, please do not hesitate to contact info@pender.ch. Additional dimensional data or Gerber layout information can be provided, if required to aid in the layout of the User's mezzanine board.

2.6 Other Auxiliary Interfaces and Circuits

2.6.1 Oscillators and Clock Inputs

The oscillator and clock scheme for the *GR718-BOARD* Board is shown in Figure 2-13.

The main oscillator providing the *SYS_CLK* for the *GR718* ASIC is a 50 MHz Crystal oscillator. To enable different oscillator frequencies to be used, a DIL socket is provided which accepts 4 pin DIL8 style 3.3V oscillator components.

Additionally, oscillators are provided as follows:

- *SPW_CLK:* DIL Socket for 100 MHz oscillator to provide a separate clock for the Spacewire interfaces
- 12MHz crystal for the FTDI interface chip

The *SYS_CLK* is also connected to the Mezzanine connector.

For more details of the internal PLL structure and clock gating features of the ASIC please refer to RD-4.

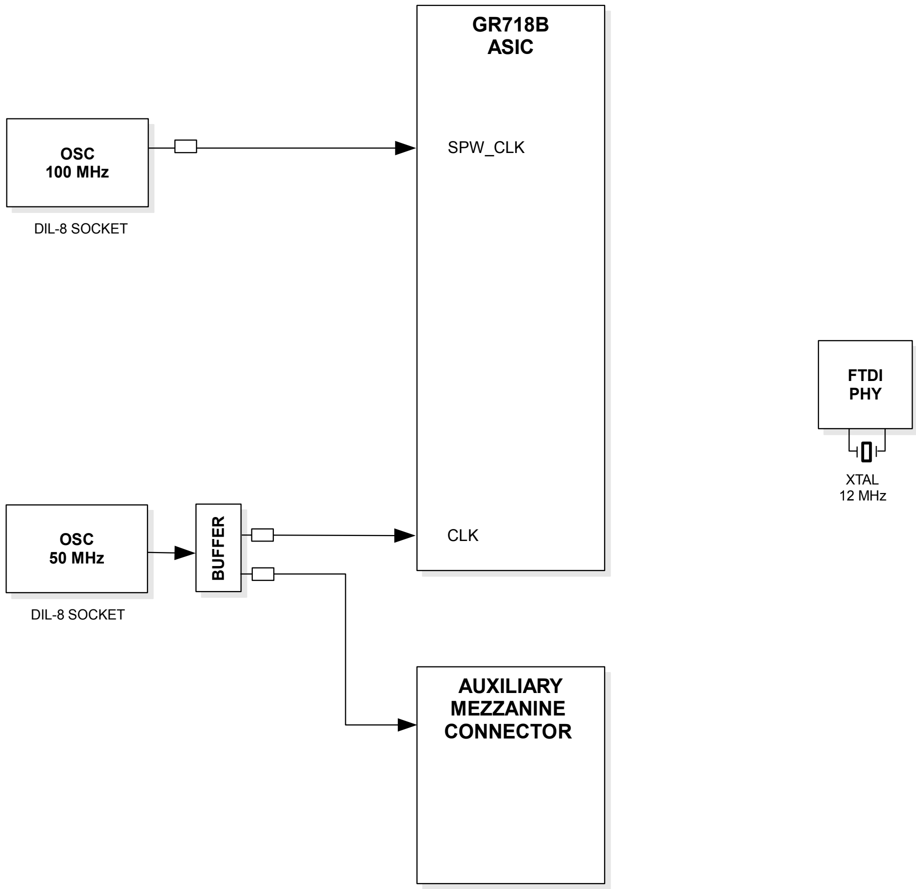

Figure 2-13: Board level Clock Distribution Scheme

2.6.2 Power Supply and Voltage Regulation

A single power supply with a +5V (nominal) is required to power the board. All other necessary voltages on the board are derived from this input using discrete Power circuits on the board (DC/DC or Linear Regulators as appropriate).

On board regulators generate the following voltages:

- +3.3V for the *GR718-BOARD* I/O voltage, interfaces and other peripherals
- +1.8V for *GR718-core* supply voltage
- +1.8V linear regulated supply for PLL

Appropriate decoupling capacitance is provided for all the supply voltages.

The Power Supply structure is comfortably dimensioned using 3A power modules (*LMZ10503*) as the basis, in order to provide for uncertainty and flexibility. The advantage of the selected DCDC power modules is their ease of implementation and the allowable input voltage range (+4.5V to +5.5V).

Input Voltage

The nominal input voltage for the board is +5V. This input voltage can be connected either to the 2.1mm Jack connector, *J11* on the board, or taken from the +5V PCI rail from the PCI Backplane. An additional power input connector *J10* is provided on the board, as an alternative to the connector *J11*. This could be useful as a more convenient connection in the situation that the board would be built in to a 'stand-alone' equipment housing.

Note: You must not apply power to the connector J10/J11 when the board is plugged into a CPCI rack.

Power Sequencing

There is no power sequencing logic implemented on this board.

The LMZ10503 begins to operate when both the VIN and EN voltages rise above their Under-voltage-lock-out and enable thresholds, respectively. A controlled soft-start eliminates inrush currents during start-up.

If required, an adjustment of the start-up sequencing could be achieved by changing the values of the Soft-start (SS) capacitors on the LMZ10503 regulators.

CPCI +/-12V Supply

The +12V and -12V (500mA max) power supply which the compact PCI can provide via the Backplane is not used on this board.

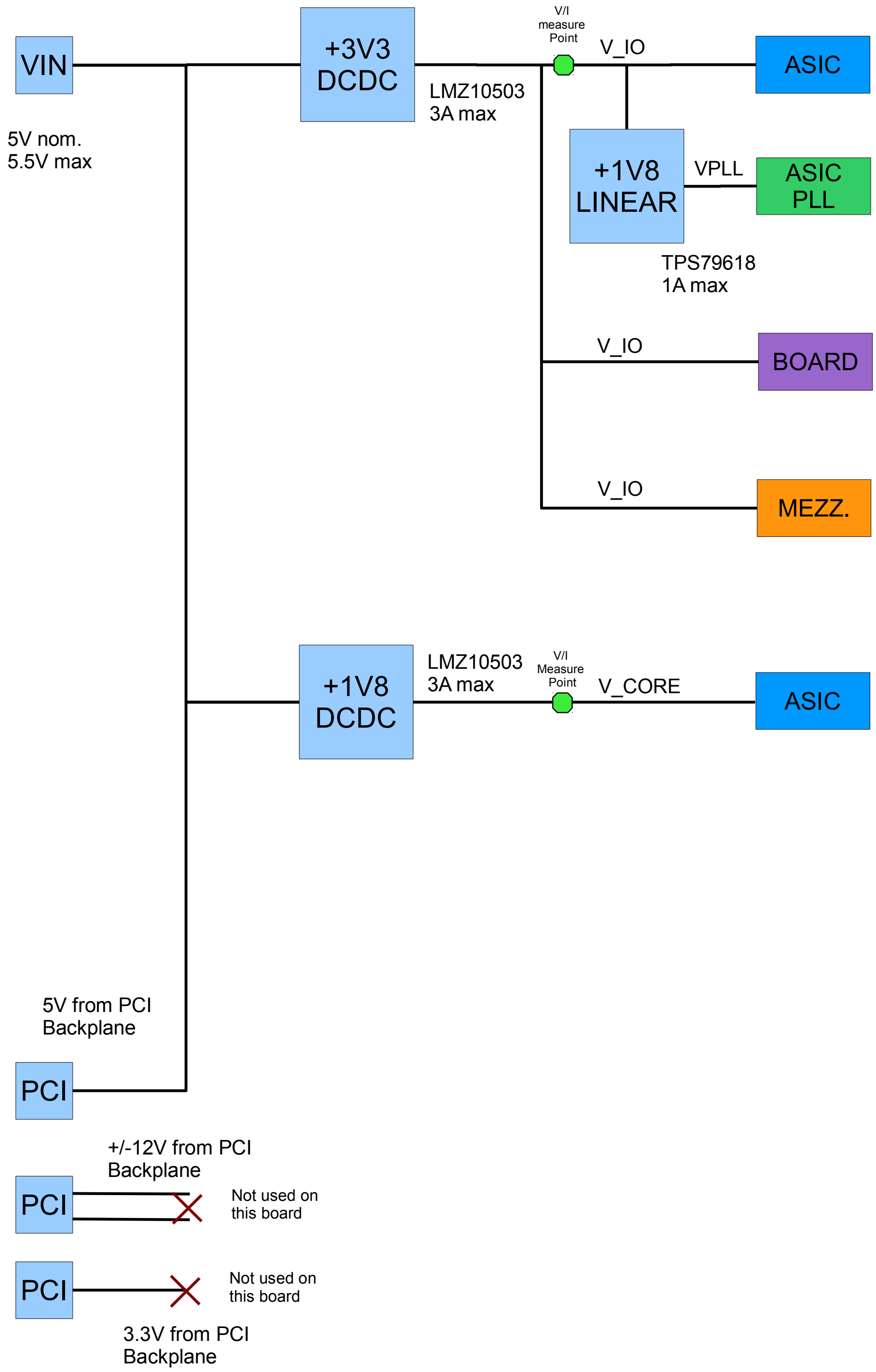

Figure 2-14: Power Regulation Scheme

2.6.3 Voltage/Current/Power Measurement

In order to enable the measurement and characterisation of power consumption of the GR718B ASIC, two measurements circuits with an I2C interface are provided as part of the Power Regulation scheme. The measurement points are represented in the figure above and use a low-resistance series resistor and a INA219 'high-side current shunt and power with I2C interface' from Texas Instruments (TI).

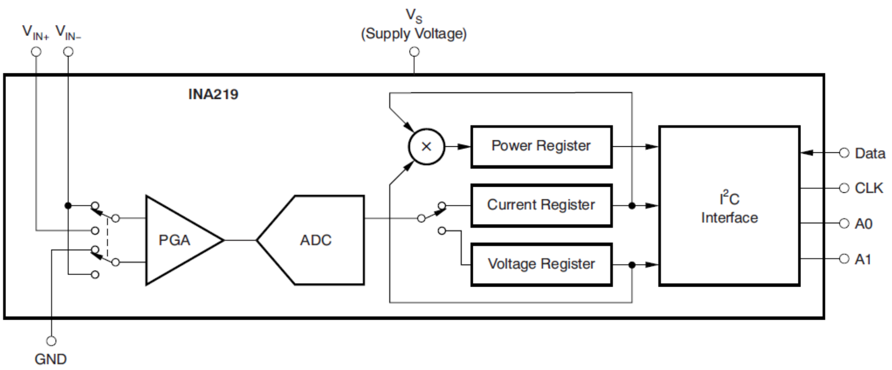

Figure 2-15: INA219 Block Diagram

The INA219 is a sophisticated device with front-end programmable gain and calibration which requires programming via its I2C interface. The I2C interface is routed to a simple 4 pin header which can be connected to the TI INA219 evaluation board and software to conveniently allow the programming and monitoring of the devices.

2.6.4 Reset Circuit and Button

A standard Processor Power Supervisory circuit (*TPS3705* or equivalent) is provided on the Board to provide monitoring of the 3.3V power supply rail and to generate a clean reset signal at power up of the Unit.

To provide a manual reset of the board, a miniature push button switch is provided on the Main PCB for the control. Additionally, connections are provided to an off-board push-button *RESET* switch on the front panel, if this is required.

2.7 PCB Design

2.7.1 Technology Table / Routing Rules

The following routing rules have been implemented for the PCB layout (In approx order of criticality)

Note: Length matching should into account the internal package length inside the ASIC in addition to the PCB trace lengths.

Interface /Signal Group	Signal Type	Constraint	Comment
SPW	LVCMOS	Characteristics	50 Ohm
	33	Track/Spacing	50/100 Ohm => depends on stack up; larger widths preferred to reduce skin effect
		Length-match	5mil (0.125mm) within pair; <200mil (5mm) within group of pairs
		Clearance	4 x Dielectric Height to other signals (ca. 0.5mm)
		Layer	Internal preferred except fanout. Minimise layer changes. Reference to DGND
SPW-TX	LVDS	Characteristics	Differential 50/100Ohm, High Speed (up to 400MHz)
		Track/Spacing	50/100 Ohm => depends on stack up; larger widths preferred to reduce skin effect
		Length-match	5mil (0.125mm) within pair; <200mil (5mm within group of pairs)
		Clearance	4 x Dielectric Height to other signals (ca. 0.5mm)
		Layer	Internal (Stripline), max 2 vias Preferred reference plane = DGND
SPW-RX	LVDS	Characteristics	Differential 50/100Ohm, High Speed (up to 400MHz)
		Track/Spacing	50/100 Ohm => depends on stack up; larger widths preferred to reduce skin effect
		Length-match	5mil (0.125mm) within pair; <200mil (5mm) within group of pairs
		Clearance	4 x Dielectric Height to other signals (ca. 0.5mm)
		Layer	Internal (Stripline), max 2 vias Preferred reference plane = DGND
SPI	LVCMOS	Characteristics	ca. 50MHz max,
	33	Track/Spacing	Non critical; 6mil typ.
		Length-match	None
		Clearance	Target >0.2mm
		Layer	Any
UART	LVCMOS	Characteristics	ca. 115200 kHz max,
	33	Track/Spacing	Non critical; 6mil/0.15mm typ.
		Length-match	None
		Clearance	Target >0.2mm

Interface /Signal Group	Signal Type	Constraint	Comment
		Layer	Any
GPIO, JTAG	LVCMOS	Characteristics	Low speed; non critical
& Other	33	Track/Spacing	Non critical; 6mil/0.15mm typ.
		Length-match	None
		Clearance	Target >0.2mm
		Layer	Any

Table 4: Technology Table /Routing Rules Summary

2.7.2 Layer Stack-up

The 'as-designed' layer stack-up is shown in Figure 2-16.

This board is an 8 layer board with nominal thickness of 1.6mm.

The PCI specification requires that the board thickness is constrained to 1.6mm +/- 0.1mm.

The design is based on a target 50 Ohm characteristic impedance for Single-Ended and 100 Ohm for Differential signals.

The resulting technology for this board is:

- *8 layer board*
- *Conventional, no blind and buried vias.*
- *0.15mm / 0.15mm trace/spacing*
- *0.5mm / 0.25mm pad/hole minimum via size*

Stackup Information:

Laye				Thicl
TOP	==================================			0.333+Plating
	PP	S0401	1080+1080	5.347(mil)
L2	==================================			1Oz
	Core	S1141	0.21	8.268(mil)
L3	==================================			1Oz
	PP	S0401	1080+2116	7.376(mil)
L4	==================================			1Oz
	Core	S1141	0.21	8.268(mil)
L5	==================================			1Oz
	PP	S0401	1080+2116	7.380(mil)
L6	==================================			1Oz
	Core	S1141	0.21	8.268(mil)
L7	==================================			1Oz
	PP	S0401	1080+1080	5.349(mil)
BOT	==================================			0.333+Plating

Finished Thickness:1.55(+0.155/-0.155) MM
Designed Thickness:1.490 MM
Material Type:S1141

Impedance Information:

Ctrl	Ref	Imp_type	Cust_req	Imp_req	FP_des	Imp_des	mask	H1	Er1	H2	Er2
L2	L1/L3	Differe	4.921/10.82	100+/-10%	4.921/10.82	99.919		8.26'	3.95	6.59'	3.65
L2	L1/L3	Single-	5.906	50+/-10%	5.500	49.809		8.26'	3.95	6.59'	3.65
L7	L6/L8	Single-	5.906	50+/-10%	5.500	49.812		8.26'	3.95	6.59:	3.65
L7	L6/L8	Differe	4.921/10.82	100+/-10%	4.921/10.82	99.924		8.26'	3.95	6.59:	3.65

Figure 2-16: Layer Stack-up

Mainly, the top and bottom layers are used only for fan-out and low speed uncritical signals (e.g. PIO signals and UART interfaces).

Internal layers are used for the high speed traces, with each internal routing layer being provided with a Ground reference plane. High speed traces are routed with a maximum via count of two, to minimise changes in routing layers.

3 Setting Up and Using the BOARD

The default status of the Jumpers on the boards is as shown in Table 5. (Other configurations may be defined by the user).

For additional information, refer to *RD-1 and RD-4*.

Jumper	Jumper Setting	Comment
JP1	Not installed	TESTEN[1..0]
JP2	Connected to front panel switch	RESET; Connected to front panel reset switch
JP3	3-5 and 4-6	SERIAL-RX; FTDI Config. => see Figure 2-8;
JP4	Not fitted	I2C SDI/SDO connection
JP5	No connection	DGND & +VIN
JP6	No connection	DGND & +3.3V
JP7	Not connected	I2C-PWR
JP8	No connection	Power SS control
J14	8-10	Connects SLVSEL to chip select of U16
S1 1-8	Middle = 'Float'	GPIO[0..7]
S2 1-8	Middle = 'Float'	GPIO[8..15]
S3 1-8	Middle = 'Float'	GPIO[16..23]
S5-1	High [1)]	SPWDIV0; Reset value for SpaceWire port's clock divisor register. See section 4 in RD-4 details.
S5-2	Low [1)]	SPWDIV1; Reset value for SpaceWire port's clock divisor register. See section 4 in RD-4 details.
S5-3	Low [1)]	SPWDIV2; Reset value for SpaceWire port's clock divisor register. See section 4 in RD-4 details.
S5-4	High [1)]	SPWDIV3; Reset value for SpaceWire port's clock divisor register. See section 4 in RD-4 details.
S5-5	Low [1)]	SPWDIV4; Reset value for SpaceWire port's clock divisor register. See section 4 in RD-4 details.
S5-6	Low [1)]	SPWDIV5; Reset value for SpaceWire port's clock divisor register. See section 4 in RD-4 details.
S5-7	High	SPILL, Enable spill-if-not-ready feature. See section 6.2.7 in RD-4 for details
S5-8	High	PNPEN; Enable SpaceWire Plug-and-Play at reset
S6-1	Low	SPWSEL0; Selects internal SpaceWire clock. See section 4 in RD-4 for details.
S6-2	Low	SPWSEL1; Selects internal SpaceWire clock. See section 4 in RD-4 for details.
S6-3	Low	SPWSEL2; Selects internal SpaceWire clock. See section 4 in RD-4 for details.
S6-4	High	GPIOSEL; Function selection for GPIO signals. See

		section 5 in RD-4 for details.
S6-5	Low	LNKSTR; Reset value for the SpaceWire ports' link-start-on-request feature. See section 6.2.10 in RD-4 for details
S6-6	Low	AUTOCON; Reset value for the SpaceWire ports' auto-disconnect feature. See section 6.2.11 in RD-4 for details.
S6-7	Low	STROUT; Enables / disables the static routing feature at reset. See section 6.2.6 in RD-4 for details.
S6-8	Low	CFGCLK; Enable accesses to configuration port from all ports. See section 6.5.1.3 in RD-4 for details
Note 1	Only applicable when internal SpaceWire clock frequency is 100Mhz. See section 4 in RD-4 more details.	

Table 5: Default Status of Jumpers/Switches

To operate the unit stand alone on the bench top, connect the +5V power supply to the Power Socket *J11* at the back of the unit. (centre-pin is +ve).

ATTENTION! To prevent damage to board, please ensure that the correct power supply voltage and polarity is used with the board.

Do not exceed +5.5V at the power supply input, as this may damage the board.

The *POWER LED's* should be illuminated indicating that the +3.3V power and +1.8V power are active.

Other LED's may illuminate depending on the DIP switch settings of the board and the corresponding operating mode in which the ASIC powers up.

To perform interrogation and debugging on the hardware it is necessary to use the Cobham Gaisler *GRMON2* debugging software, installed on a host PC (as represented in Figure 2-12). Please refer to the *GRMON2* documentation for the installation of the software on the host PC (Linux or Windows), and for the installation of the associated hardware dongle.

To perform debugging, a link from the Host computer to the DSU interface of the board is necessary. As described in section 2.4.7 this requires the host computer to be connected to the JTAG-DCL link via the FTDI interface (connector J1)

More information on the usage, commands and debugging features of *GRMON2* , is given in the *GRMON2 Users Manuals* and associated documentation.

4 Interfaces and Configuration

4.1 List of Connectors

Name	Function	Type	Description
J1	FTDI-USB	USB-MINI-AB	Configurable serial to USB I/F via FTDI converter acc. §2.4.4
J2	GPIO[11..0]	2x13 pin 0.1" Header	Pin connections for PIO signals 0 to 11 & AUXTICKIN
J3	GPIO[23..12]	2x13 pin 0.1" Header	Pin connections for PIO signals 12 to 23 & AUXTICKOUT
J4	3-port SPW	SAMTEC-40pin	SPW 1/2/3; Connects with Flexprint to 3 MDM9S conn.
J5	3-port SPW	SAMTEC-40pin	SPW 4/5/6; Connects with Flexprint to 3 MDM9S conn.
J6	3-port SPW	SAMTEC-40pin	SPW 7/8/9; Connects with Flexprint to 3 MDM9S conn.
J7	3-port SPW	SAMTEC-40pin	SPW 10/11/12; Connects with Flexprint to 3 MDM9S conn.
J8	3-port SPW	SAMTEC-40pin	SPW 13/14/15; Connects with Flexprint to 3 MDM9S conn.
J9	3-port SPW	SAMTEC-40pin	SPW 16/17/18; Connects with Flexprint to 3 MDM9S conn.
J10	POWER-IN'	Mate-N-Lok 4pin	Alternative power input for 4 pin IDE style connector
J11	POWER-IN	2.1mm center +ve	+5V DC power input connector
J12	MEZZANINE	AMP 5-177984-5	Control/Status signals for Auxiliary Mezzanine
J13	UART-RS232	2x5 pin 0.1" Header	Header for Serial UART signals
J14	SPI	2x6 pin 0.1" Header	Header for User SPI connections
J15	IRQ-LK	2x2 pin 0.1" Header	Header for IRQ and LOCK signals
J16	SYS-CLK	SMA-jack	Coaxial connector for injecting alternative MAN-CLK
J17	SPW-CLK	SMA-jack	Coaxial connector for injecting alternative SPW-CLK
J18	SPI-ADCDAC	2x10 pin 0.1" Header	Header for SPI ADC/DAC circuit
J19	HDR-DIP	2x10 pin 0.1" Header	Header for ribbon cable with Front panel DIP switch
CPCI-J1	CPCI	CPCI Type A	CPCI connector

Table 6: List of Connectors

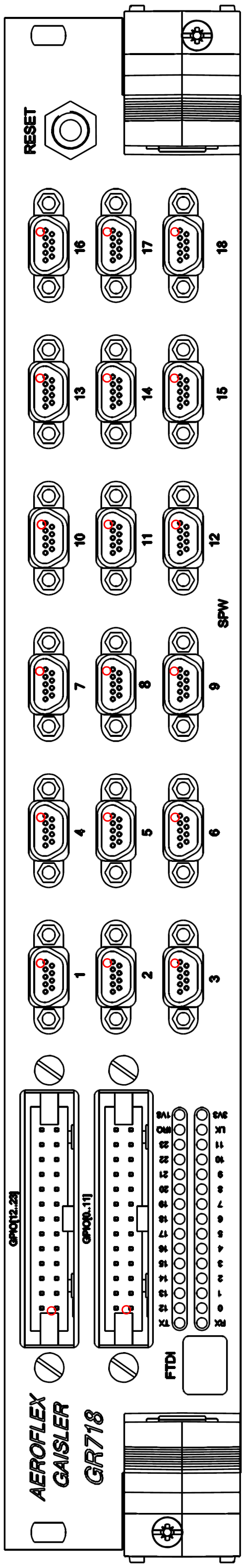

Figure 4-1: Front Panel View (pin 1 marked with red circle)

Pin	Name	Comment
1	VBUS	+5V (from external host)
2	DM	Data Minus
3	DP	Data Plus
4	ID	Not used
5	DGND	Ground

Table 7: J1 USB type Mini AB connector – FTDI Dual Serial Communication Link

FUNCTION	CONNECTOR PIN		FUNCTION
GPIO0	1	2	DGND
GPIO1	3	4	DGND
GPIO2	5	6	DGND
GPIO3	7	8	DGND
GPIO4	9	10	DGND
GPIO5	11	12	DGND
GPIO6	13	14	DGND
GPIO7	15	16	DGND
GPIO8	17	18	DGND
GPIO9	19	20	DGND
GPIO10	21	22	DGND
GPIO11	23	24	DGND
AUXTICKIN	25	26	DGND

Table 8: J2 PIO Header Pin out – GPIO[0..11]

FUNCTION	CONNECTOR PIN		FUNCTION
GPIO12	1	2	DGND
GPIO13	3	4	DGND
GPIO14	5	6	DGND
GPIO15	7	8	DGND
GPIO16	9	10	DGND
GPIO17	11	12	DGND
GPIO18	13	14	DGND
GPIO19	15	16	DGND
GPIO20	17	18	DGND
GPIO21	19	20	DGND
GPIO22	21	22	DGND
GPIO23	23	24	DGND
AUXTICKOUT	25	26	DGND

Table 9: J3 PIO Header Pin out – GPIO[12..23]

Pin	Name	Comment
1	DIN0+	Data In +ve
6	DIN0-	Data In -ve
2	SIN0+	Strobe In +ve
7	SIN0-	Strobe In -ve
3	SHIELD	Inner Shield
8	SOUT0+	Strobe Out +ve
4	SOUT0-	Strobe Out -ve
9	DOUT0+	Data Out +ve
5	DOUT0-	Data Out -ve

Table 10: SPW-1 – SPW-18 interface connections (18x) on Front Panel MDM connectors

Pin	Name	Comment
1	Not connected	Not used
2	GND	Ground
3	GND	Ground
4	+5V	+5V

Table 11: J10 POWER – External Power Connector

Pin	Name	Comment
+VE	+5V	Inner Pin, 5V
-VE	GND	Outer Pin Return

Table 12: J11 POWER – External Power Connector

FUNCTION	FPGA PIN	CONNECTOR PIN		FPGA PIN	FUNCTION
DGND		1	120		DGND
+5V		2	119		+5V
DGND		3	118		DGND
-12V		4	117		-12V
DGND		5	116		DGND
+12V		6	115		+12V
DGND		7	114		DGND
		8	113		
		9	112		
+3.3V		10	111		+3.3V
DGND		11	110		DGND
GPIO0		12	109		GPIO1
GPIO2		13	108		GPIO3
GPIO4		14	107		GPIO5
GPIO6		15	106		GPIO7
GPIO8		16	105		GPIO9
GPIO10		17	104		GPIO11
GPIO12		18	103		GPIO13
GPIO14		19	102		GPIO15
+3.3V		20	101		+3.3V
DGND		21	100		DGND
GPIO16		22	99		GPIO17
GPIO18		23	98		GPIO19
GPIO20		24	97		GPIO21
GPIO22		25	96		GPIO23
		26	95		
		27	94		
		28	93		
RX		29	92		TX
+3.3V		30	91		+3.3V
DGND		31	90		DGND
AUTODCONN		32	89		IRQ
CFGLOCK		33	88		LOCK
PNPEN		34	87		SPILL
TESTEN0		35	86		TESTEN1
STROUTEEN		36	85		GPIOSEL
		37	84		LNKSTREQ
		38	83		
		39	82		
+3.3V		40	81		+3.3V
DGND		41	80		DGND
SPWCLKDIV0		42	79		SPWCLKDIV1
SPWCLKDIV2		43	78		SPWCLKDIV3
SPWCLKDIV4		44	77		SPWCLKDIV5
SPWCLKSEL0		45	76		SPWCLKSEL1
SPWCLKSEL2		46	75		
		47	74		
AUXTICKIN		48	73		AUXTICKOUT
		49	72		
+3.3V		50	71		+3.3V
DGND		51	70		DGND
SPI_MISO		52	69		TMS
SPI-MOSI		53	68		TCK
SPI_CLK		54	67		TDF
SPI_SLVSEL		55	66		TDO
		56	65		
		57	64		MEZZ_CK
		58	63		
RESETN		59	62		
DGND		60	61		DGND

Table 13: J12 -Status/Control signals for Auxiliary Mezzanine

(see note in §2.5 on pin-numbering)

FUNCTION	ASIC pin	CONNECTOR PIN		FUNCTION
nc		1	6	nc
TXD		2	7	nc
RXD		3	8	nc
nc		4	9	nc
DGND		5	10	Not used

Table 14: J13 -UART Header for Serial UART signals (RS232)

(Note: This can be connected with a 1:1 ribbon cable connection to a DSUB9 connector for a standard RS232 serial cable connection)

FUNCTION	ASIC pin	CONNECTOR PIN		ASIC pin	FUNCTION
SPI_SLVSEL1		1	2		SPIC_MISO
SPI_SLVSEL2		3	4		SPI_MOSI
SPI_SLVSEL3		5	6		SPI_SCK
SPI_SLVSEL4		7	8		SPI_SLVSEL
SPI_SLVSEL5		9	10		SPI_SLVOB
DGND		11	12		+3V3

Table 15: J14 SPI Header for User SPI interface

FUNCTION	ASIC pin	CONNECTOR PIN		ASIC pin	FUNCTION
IRQ		1	2		DGND
LOCK		3	4		DGND

Table 16: J15 Header for IRQ & LOCK signals

Pin	Name	Comment
centre	SPWCLK	SPW Clock
ground	GND	Ground/Return

Table 17: J16 SMA – SPW-Clock

(Note: To use this SMA connector to inject a clock signal, remove the Oscillator from the socket)

Pin	Name	Comment
centre	CLK	Main Clock
ground	GND	Ground/Return

Table 18: J17 SMA – SYS-Clock

(Note: To use this SMA connector to inject a clock signal, remove the Oscillator from the socket)

FUNCTION	CONNECTOR PIN		FUNCTION
DAC0	1	2	DGND
DAC1	3	4	DGND
DAC2	5	6	DGND
DAC3	7	8	DGND
ADC0	9	10	DGND
ADC1	11	12	DGND
ADC2	13	14	DGND
ADC3	15	16	DGND
INTR	17	18	DGND
GPIO23	19	20	DGND

Table 19: J18 Header for SPI ADC/DAC

FUNCTION	CONNECTOR PIN		FUNCTION
SPWCLKDIV0	1	2	SPWCLKDIV1
SPWCLKDIV2	3	4	SPWCLKDIV3
SPWCLKDIV4	5	6	SPWCLKDIV5
SPILL	7	8	PNPEN
SPWCLKSEL0	9	10	SPWCLKSEL1
SPWCLKSEL2	11	12	GPIOSEL
LNKSTREQ	13	14	AUTODCONN
STROUTEEN	15	16	CFGLOCK
+3.3V	17	18	+3.3V
DGND	19	20	DGND

Table 20: J19 Header for Front Panel dip switches (option)

4.2 List of Oscillators, Switches and LED's

Name	Function	Description
X1	OSC_MAIN	Oscillator for main ASIC clock, 3.3V, DIL8 socket, 50 MHz
X2	OSC_SPW	Oscillator for SPW interfaces, 3.3V, DIL8 socket, 200 MHz (TBC)
Y1	XTAL_FTDI	Crystal for FTDI interface, 12MHz

Table 21: List and definition of Oscillators and Crystals

Name	Function	Description
D1	UART RX/TX	Dual LED indicator for UART RX & TX (when operating through FTDI)
D2-D13	GPIO[23..0]	Dual LED indicators for GPIO[23..0]
D14	PWR / LOCK	Dual LED indicator for 'LOCK' and 'IRQ'
D15	PWR / LOCK	Dual LED indicator for 'POWER 3.3V' and 'POWER 1.8V'

Table 22: List and definition of PCB mounted LED's

Name	Function	Description
S1	GPI0[7..0]	8 pole double throw DIP switch; can be set to 'pull-up', 'pull-down' or 'float'
S2	GPIO[15..8]	8 pole double throw DIP switch; can be set to 'pull-up', 'pull-down' or 'float'
S3	GPIO[23..16]	8 pole double throw DIP switch; can be set to 'pull-up', 'pull-down' or 'float'
S4	RESET	Push button RESET switch
S5	ASIC-Control-1	8 pole DIP switch; Straps ASIC pins high/low - see table below
S6	ASIC-Control-2	8 pole DIP switch; Straps ASIC pins high/low - see table below

Table 23: List and definition of Switches

FUNCTION	ASIC pin	OPEN	SWITCH	CLOSED
SPWDIV0		'1'	1	'0'
SPWDIV1		'1'	2	'0'
SPWDIV2		'1'	3	'0'
SPWDIV3		'1'	4	'0'
SPWDIV4		'1'	5	'0'
SPWDIV5		'1'	6	'0'
SPILL		'1'	7	'0'
PNPEN		'1'	8	'0'

Table 24: DIP Switch S5 'ASIC-Control-1' definition

FUNCTION	ASIC pin	OPEN	SWITCH	CLOSED
SPWSEL0		'1'	1	'0'
SPWSEL1		'1'	2	'0'
SPWSEL2		'1'	3	'0'
GPIOSEL		'1'	4	'0'
LNKSTR		'1'	5	'0'
AUTOCON		'1'	6	'0'
STROUT		'1'	7	'0'
CFGCLK		'1'	8	'0'

Table 25: DIP Switch S6 'ASIC-Control-2' definition

4.3 List of Jumpers

Name	Function	Type	Description
JP1	TESTEN[1..0]	2x2 pin 0.1” Header	Inset jumper 1-2 to set TESTEN0 and,/or 3-4 for TESTEN1 to be set 'high'
JP2	RESET	2 pin 0.1” Header	Pins for external front panel RESET switch
JP3	SERIAL-RX/TX	8 pin 0.1” Header	Configuration options for FTDI JTAG/UART I/F
JP4	SDI/SDO	2 pin 0.1” Header	Configuration options for I2C power measure I/F
JP5	+VIN	1x2 0.1”Header	Test/Power header (Pin 1 = DGND, Pin2 = +5V)
JP6	+3.3V	1x2 0.1”Header	Test/Power header (Pin 1 = DGND, Pin2 = +3.3V)
JP7	I2C-PWR	2x2 pin 0.1” Header	I2C Test Header for Power Measurement testing
JP8	PWR-EN	2x2 pin 0.1” Header	Header for auxiliary DCDC ON/Off control

Table 26: List and definition of PCB Jumpers
(for details refer to schematic, RD 1)

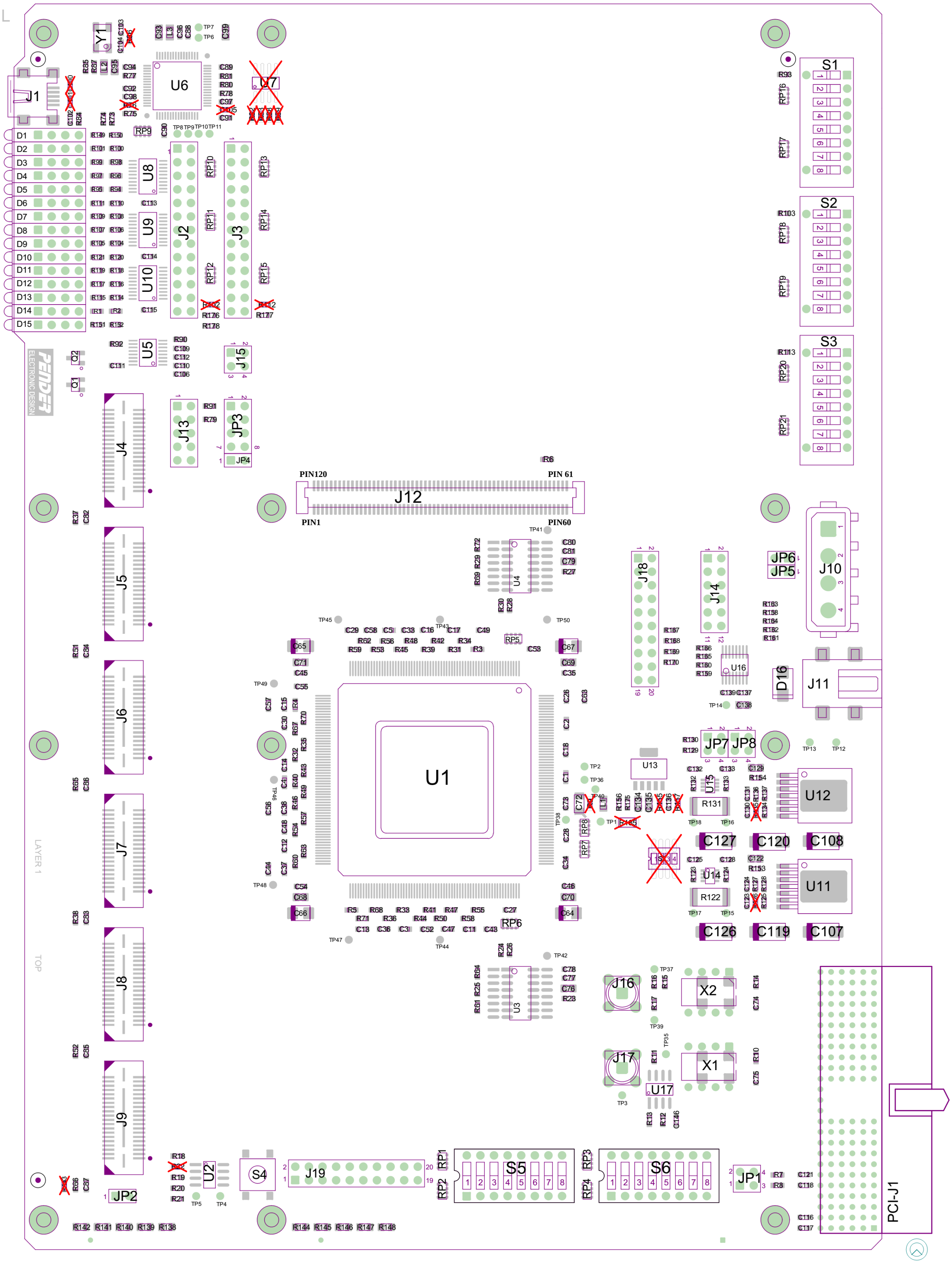

Figure 4-2: PCB Top View

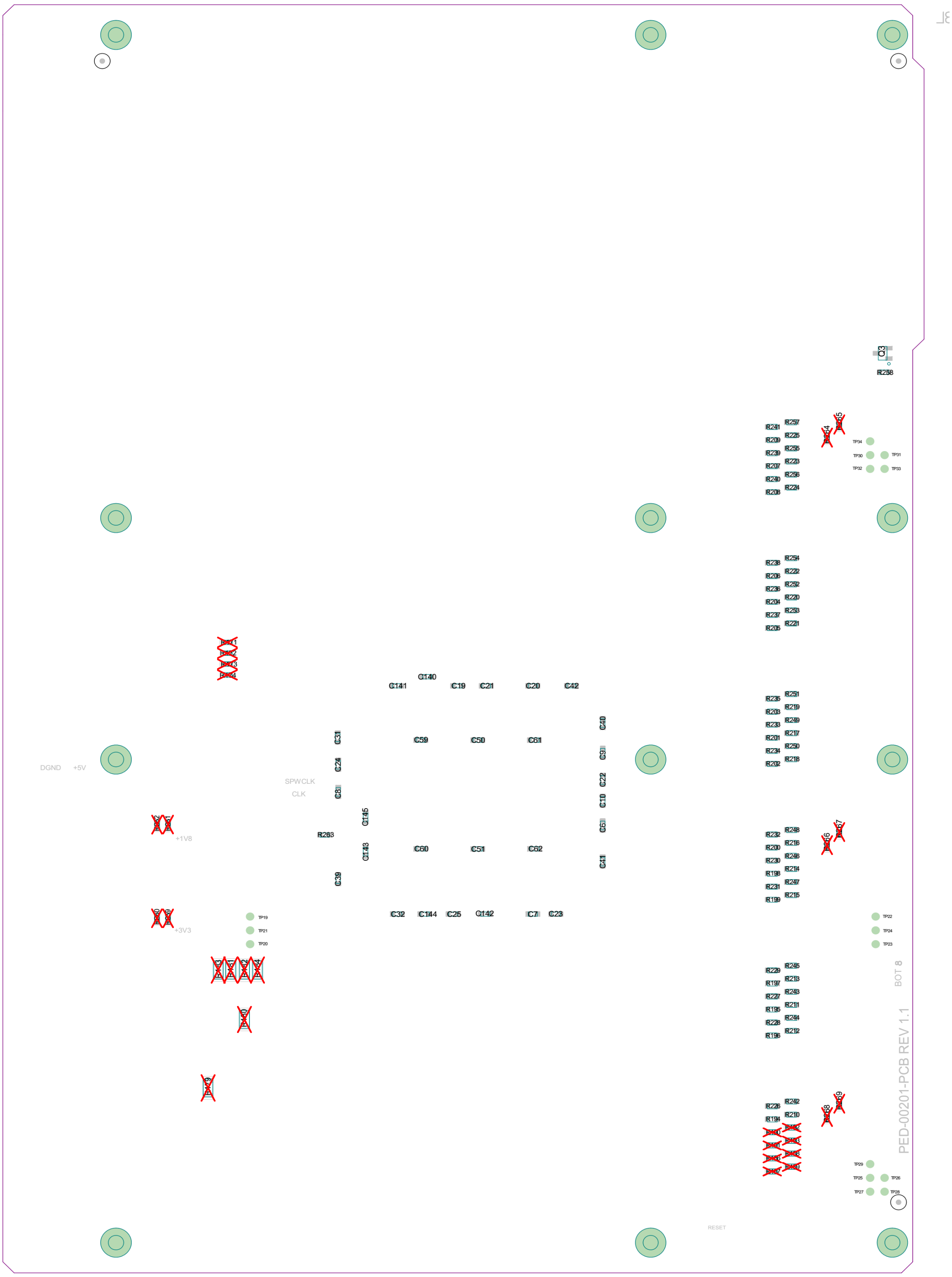

Figure 4-3: PCB Bottom View

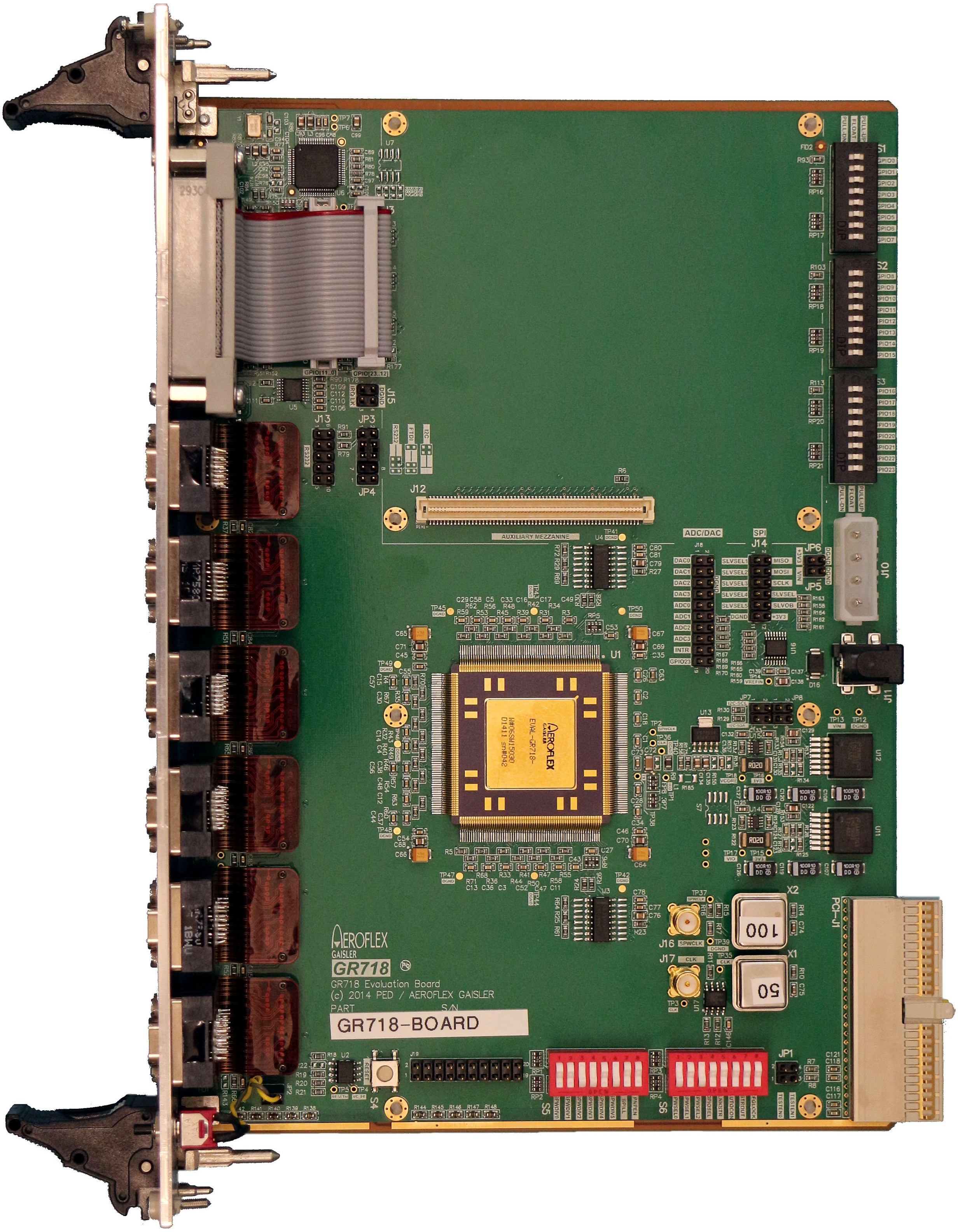

Figure 4-4: PCB Top View (Photo)

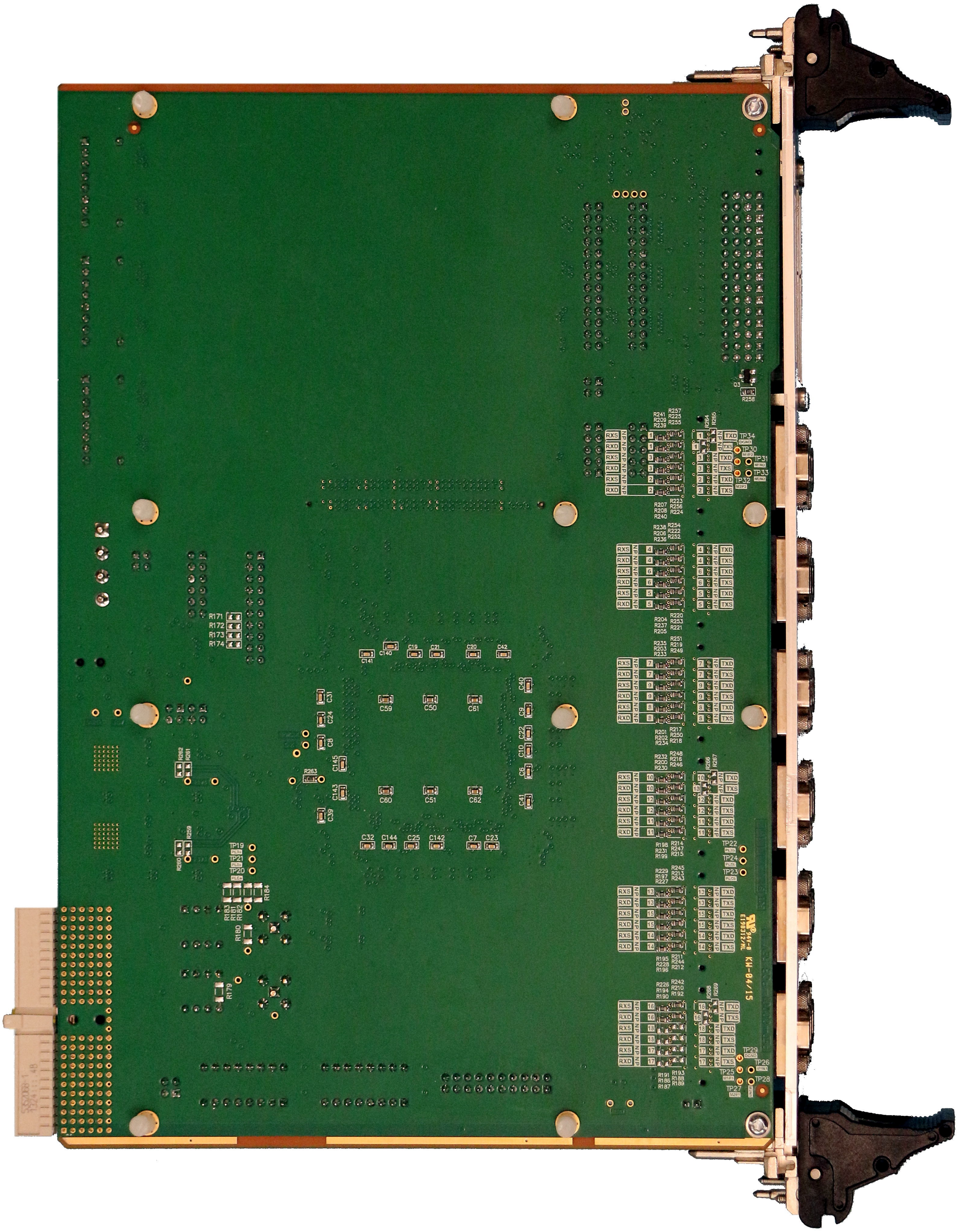

Figure 4-5: PCB Bottom View (Photo)

5 Change Record

Issue	Date	Section / Page	Description
0.0	2015-10-12	All	Draft Issue
0.1	2016-01-23	All	Draft Issue. New Cobham Gaisler template
1.1	2016-02-26	All	Updated after prototype hardware
1.2	2016-04-12	Table 5	Correct jumper setting for JP11
1.3	2016-04-12	All	Corrected device name and version and updated default values in Table 5
1.4	2018-03	Table 11	Corrected external power connector

Cobham Gaisler AB
Kungsgatan 12
411 19 Göteborg
Sweden
www.cobham.com/gaisler
sales@gaisler.com
T: +46 31 7758650
F: +46 31 421407